An Ultra-fast Multi-level MoTe$_2$-based RRAM

F. Zhang[1], H. Zhang[2,3], P.R. Shrestha[2,3], Y. Zhu[1], K. Maize[1], S. Krylyuk[2,3], A. Shakouri[1], J.P. Campbell[3], K.P. Cheung[3], L.A. Bendersky[3], A.V. Davydov[3] and J. Appenzeller[1*]

[1]Purdue University, West Lafayette, IN, USA, *email: appenzeller@purdue.edu,
[2]Theiss Research, Inc., La Jolla, CA, USA, [3]National Institute of Standards and Technology, Gaithersburg, MD, USA,

Abstract — We report multi-level MoTe$_2$-based resistive random-access memory (RRAM) devices with switching speeds of **less than 5 ns** due to an electric-field induced 2H to 2H$_d$ phase transition. Different from conventional RRAM devices based on ionic migration, the MoTe$_2$-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our MoTe$_2$-based RRAM devices allow faster switching due to a transition between *two* crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications. Multi-level stable states and synaptic devices were realized in this work, and operation of the devices in their low-resistive, high-resistive and intrinsic states was quantitatively described by a novel model.

I. INTRODUCTION

RRAM has promises of being an emerging technology due to its potential scalability, high operation speed, high endurance and ease of process flow. However, reliable and repeatable operation is a potential challenge in future applications since switching involves the uncontrollable motion of individual atoms. In this work, we present a new switching mechanism for MoTe$_2$-based RRAM. An electric field induces the phase transition from the stable semiconducting 2H phase to a more conductive 2H$_d$ phase, which provides a potential path towards better stability. The newly formed 2H$_d$ is structurally close to the 2H phase, which holds the promise for faster switching if compared with the significant migration of ions in conventional RRAM [1] or the amorphous-to-crystalline transition in PCM [2] (see Fig.1). Initial pulse measurements show impressive switching speed of less than 5 ns. Moreover, multi-level states can be programmed into the devices by applying proper set/reset voltages, which allows to gradually changing the device resistance with multiple pulses, creating a "synaptic device".

II. SWITCHING IN MoTe$_2$ RRAM DEVICES

Fig. 1 illustrates the advantages of this new type MoTe$_2$-based RRAM as compared to conventional RRAM and PCM due to switching by an electric-field induced phase transition. Fig. 2(a) shows schematically a vertical MoTe$_2$ device. First, a bottom electrode Ti/Au (10 nm/25 nm) was deposited onto a 90 nm silicon dioxide (SiO$_2$) layer covering a highly doped silicon wafer. Next, MoTe$_2$ (2D Semiconductor) layers were exfoliated onto this electrode using standard scotch tape techniques, followed by thermal evaporation of 55 nm SiO$_2$ insulating layer. The device fabrication was finished by the deposition of a Ti/Ni (35 nm/50 nm) top electrode. Different

from previously reported CVD grown 2D material based RRAM devices [3,4] whose operation is mediated by uncontrollable defects/grain boundaries in the device structure, our active material is a single-crystalline layer, where the observed RRAM behavior is due to the intrinsic properties of MoTe$_2$. Fig. 2(b) shows an AFM image of a MoTe$_2$ vertical device. The active region is about 0.1 μm^2. Fig. 3(a) displays I-V curves of a pristine device, the device forming process and successive cycling through its high resistive state (HRS) and low resistive state (LRS). Stable and reproducible bipolar RRAM behavior was observed. Fig. 3(b) shows the I-V curves for MoTe$_2$ devices with different layer thicknesses, and Fig. 3(c) summarizes how the forming and set voltages scale with the MoTe$_2$ layer thickness.

Thermoreflection microscope images were acquired to map the location of the filament on the device after forming. Surface temperature maps with 50 mK temperature resolution and submicron (diffraction limited) spatial resolution can be acquired within a few minutes [5]. Fig. 4(a) and (b) show self-heating hotspots on the nickel electrode surface superimposed with optical images for two representative devices, indicating the position of the filaments. The occurrence of a single hotspot for each device with characteristic hotspot full-width-at-half-maximum of ~ 200 nm is consistent with joule self-heating from a source as small as a MoTe$_2$ filament. In six out of eight devices imaged the hotspot was located at the edge or corner of the active region as can be seen in Fig. 4(a) and (b). We speculate that this preferential occurrence is a result of stronger electric fields at "sharp" topological features due to patterning during the fabrication that enhances the filament formation. Fig. 4(c) shows the calibrated temperature change map for the hotspot in device (b). The detected temperature change on the filament portion is ~ 15 K.

In order to understand the filament formation mechanism in MoTe$_2$, scanning transmission electron microscopy (STEM) of cross-sectional samples was utilized. As Fig. 5 shows, in the LRS, a distorted 2H$_d$ phase was identified in the regions extending vertically throughout the MoTe$_2$ layer. The 2H$_d$ phase was identified as a distorted modification of the 2H structure – a transient state with atoms displaced to the sites of a lower symmetry, but still within atomic arrangements of the 2H structure. A detailed analysis of the structure can be found in ref. [6]. Fig. 6 shows an energy dispersive spectrometry (EDS) scan along the filament region of a device in its LRS. Almost no Ti and Au signals were detected within the filament, which – in particular when also considering the unavoidable ion-milling contamination during FIB sample preparation – implies that the switching mechanism is *not* related to the migration of metal ions. To further confirm this point, graphene was used to replace the metal top and bottom electrodes. Fig. 7 shows the "typical" bipolar RRAM behavior

observed here in a Graphene-MoTe$_2$-Graphene device. Note that this is the first demonstration of an entirely 2D materials-based RRAM. Based on previous studies [7], graphene is a good diffusion barrier for metal ions. This 2D RRAM excludes completely the possibility of migration of metal ions as a source for the resistive switching observed by us. Based on these results, an electric-field induced phase transition from 2H to a more conductive 2H$_d$ state is believed to be responsible for the RRAM behavior in vertical MoTe$_2$ devices.

III. A PHYSICAL MODEL

To fully understand the vertical transport through the pristine, LRS and HRS states in MoTe$_2$ devices and to explore the properties of the new 2H$_d$ phase, a physical model was constructed. The barrier height Φ_{2H} and Φ_{2Hd} shown in figure 8(a) were extracted by utilizing the numerical model from ref. [8]. In this model, two different transport mechanisms are considered: thermal diffusion at low voltages and Fowler-Nordheim (FN) tunneling at higher voltages, as illustrated for a pristine data set in Fig. 8(b). In our model the 2H phase has a larger barrier height than the 2H$_d$ phase as evident when their current values in the low voltage range are compared. An excellent fit can be obtained for the pristine I-V characteristics (Fig. 8(b)), as well as for the LRS and HRS (Fig. 8(c)) by employing the band diagrams and parameters shown in Fig. 8(a). In the pristine state, the MoTe$_2$ is in its 2H phase with a large barrier height of $\Phi_{2H} = 0.38$ eV. On the other hand, in the LRS, a filament of 2H$_d$ was created through the setting process with an extracted barrier height of $\Phi_{2Hd} \approx 0.07$ eV. The HRS is characterized by formation of the 2H/2H$_d$ heterojunction due to rupture of the 2H$_d$ filament during the reset process. The thickness of newly formed 2H segment in the filament can be estimated to be $\sim$ 1.8nm. Thus, the simulation results are consistent with the notion that a new semiconducting 2H$_d$ state with a smaller barrier height is formed during the set process that is responsible for the higher conductivity of the LRS compared with the HRS.

IV. PERFORMANCE STUDY AND PULSE MEASUREMENTS

A. Performance study

Fig. 9 illustrates the pulse switching behavior in MoTe$_2$ based RRAM devices. The pulse width is 80 μs. By applying set/reset pulses, the device can switch between the LRS and HRS. Fig. 9(c) shows the read out current per cycle in the LRS and HRS. Fig. 9(d) is a retention measurement. All performance studies indicate stable and reproducible RRAM behavior.

B. Pulse measurements

To test the switching speed of our MoTe$_2$ RRAM devices, the experimental measurement setup shown in the inset of Fig. 10(b) was utilized. The current through the device was measured using a 50 Ω termination at the oscilloscope [9]. Note that no current compliance was used in this setup. The switching was controlled by varying the pulse width or pulse amplitude. A current and voltage versus time (t) plot of one such SET operation is shown in Fig. 10(a). The full width at half max (FWHM) of the applied voltage pulse is 5 ns. Fig.

10(b) shows the same data as in Fig. 10(a) but plotted as the current versus voltage. This clear change in resistance during the 5 ns voltage pulse is further evidence that the switching speed in MoTe$_2$ based RRAM is less than 5 ns.

The devices were reset (switched OFF) using negative pulses. Multiple pulses were required for a gradual reset process. Fig. 10(c) shows 10 pulses used to reset the device. Current versus voltage plots of cycle 1 (1st pulse), cycle 5 (5th pulse) and cycle 10 (10th pulse) are shown in Fig. 10(d). The gradual resistance change is a desirable feature for neuromorphic computing. Fig. 11 shows the characteristics of a device that was programmed by a series of positive pulses (1.1 V, 80 μs) followed by a series of negative voltage pulses (-1.2 V, 80 μs). The resistance of the MoTe$_2$ device gradually decreased and increased, which is similar to the potentiation and depression of biological synapses.

By carefully tuning the set/reset voltages, multi-level states can be programmed into the devices. Fig. 12(a) shows stable resistive states after various short (80 μs) and long (560 μs) voltage pulses that were read at a 0.2 V level. Long pulses result in a more substantial change (training) of the resistive state of the system. Fig. 12(b) shows the switch on/off behavior in each state. All the pulse measurements hint at an additional application space of this class of vertical TMD devices in the realm of neuromorphic computing.

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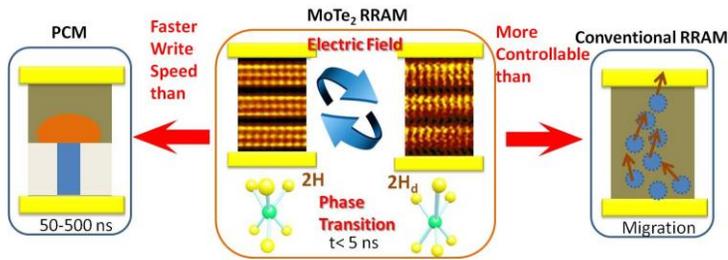
Fig. 1. Highlight features of the MoTe₂ based RRAM.

Fig. 2. (**a**) Schematic diagram of a vertical metal/MoTe₂/metal device. (**b**) AFM image of a vertical MoTe₂ device.
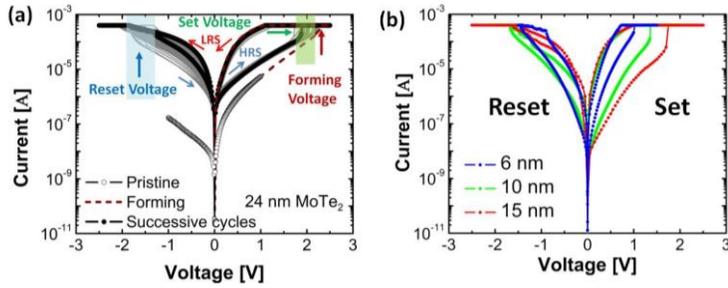
Fig. 3. (**a**) I-V curves of a 24 nm MoTe₂ device with an active area of 330 nm x 500 nm. 40 cycles are shown in the grey line curves. Current compliance is set to 400 µA. (**b**) I-V curves of vertical MoTe₂ RRAM devices from 6 nm, 10 nm, and 15 nm MoTe₂ layers with active areas of 502 nm x 360 nm, 522 nm x 330 nm and 500 nm x 330 nm respectively. (**c**) Forming/Set voltage values scale with the MoTe₂ thickness.
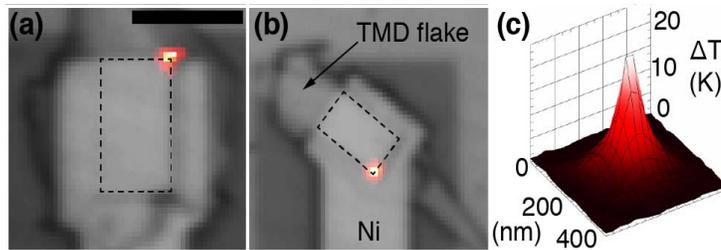
Fig. 4.(**a-b**) Thermoreflectance images showing the location of the filament. The scale bar is 5 µm. (**c**) The calibrated temperature change map for the filament in the device (**b**).

Fig.5. (**a**) HAADF-STEM image showing the cross-section of a MoTe₂ device. Higher magnification HAADF image from the region defined by the blue/red box in (**a**) showing (**b**) 2H and (**c**) a distorted structure (2H_d) taken along the $[110]_{2H}$ zone-axis. (**d**) Corresponding nano-beam diffraction pattern taken from the distorted 2H_d area.
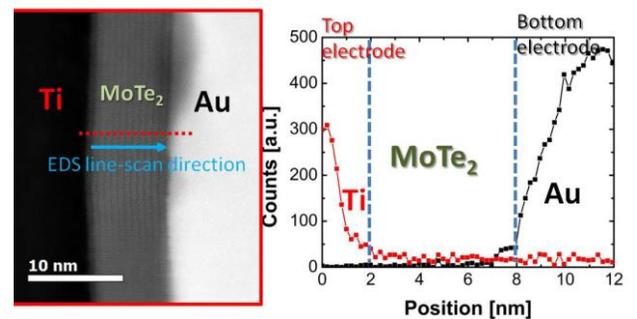
Fig. 6. EDS line-scan analysis of the filament region of a device in its LRS. Little Ti/Au signals were detected in the filament region due to ion-milling contamination during sample preparation.

Fig. 7. (**a**) Schematic and (**b**) optical images of a Graphene-MoTe₂-Graphene device. (**c**) I-V curve of the RRAM device in (**b**).
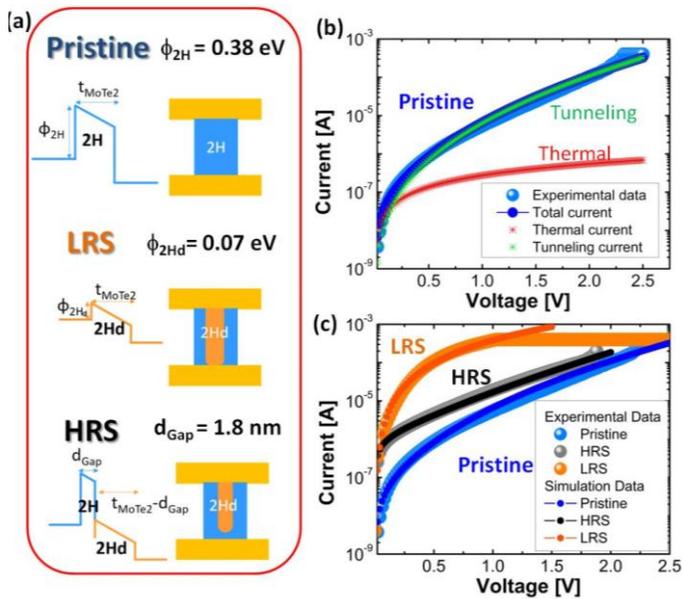
Fig. 8. (**a**) Schematic band diagrams of the RRAM in its various states. (**b**) Experimental and simulation data of a pristine device. (**c**) Experimental and simulation data for the LRS, HRS and pristine state.

Fig. 9. (**a**) DC characteristic of a 7 nm thick $MoTe_2$ layer RRAM device. (**b**) shows the various current levels after pulse switching. (**c**) Current versus cycle in the LRS and HRS at a read voltage of 0.3 V. Current compliance is set to 400 µA. (**d**) Retention of the HRS and LRS for a 15 nm thick $MoTe_2$ RRAM device. Current compliance is set to 1.2 mA.

Fig. 10. (**a**) I/V vs. time plot showing switching of the device within a 5 ns voltage pulse. (**b**) I-V plot of the data shown in (**a**) to show the change in resistance during the applied pulse. The inset figure displays the experimental setup for the pulse measurement. (**c**) I/V vs. t plot of 10 reset pulses. (**d**) I-V plot of data plotted in (**c**) of pulses 1, 5 and 10.
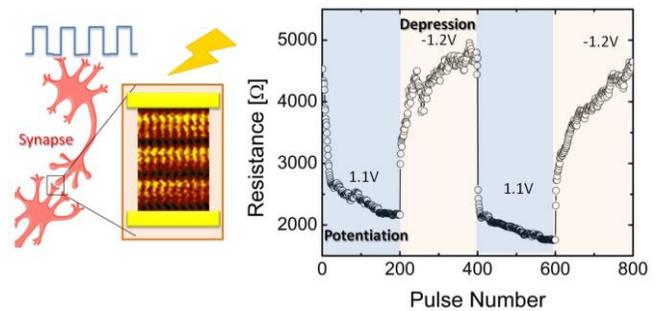
Fig. 11. Synaptic device from an $MoTe_2$ RRAM.
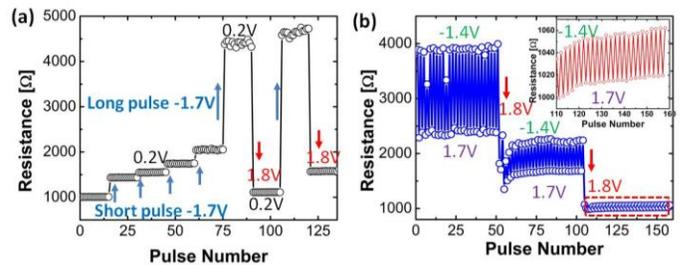
Fig. 12. (**a**) Multiple stable states of a device after various set and reset voltage pulses had been applied. Read out occurs at a voltage of 0.2 V. Every state is characterized by 15 subsequent read outs. A short pulse (80 µs) and longer pulse (560 µs) of a reset voltage of -1.7 V result in different changes of the resistance. (**b**) Multi-level characteristics of a vertical $MoTe_2$ device. Each level exhibits stable switch on/off at set/reset voltages of 1.7 V and -1.4 V respectively. A third state can be "dialed in" through yet another 1.8 V pulse. The inset figure is the zoom-in of the red dashed part.