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ARTICLE

Complementary Black Phosphorus Tunneling Field-Effect Transistors

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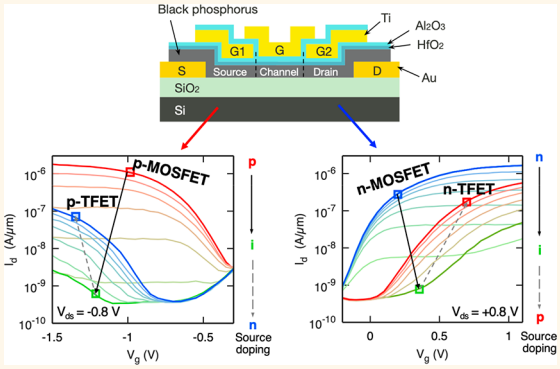
Supporting Information

ABSTRACT: **Band-to-band tunneling field-effect transistors (TFETs) have emerged as promising candidates for low-power integration circuits beyond conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) and have been demonstrated to overcome the thermionic limit, which results intrinsically in subthreshold swings of at least 60 mV/dec at room temperature. Here, we demonstrate complementary TFETs based on few-layer black phosphorus, in which multiple top gates create electrostatic doping in the source and drain regions. By electrically tuning the doping types and levels in the source and drain regions, the device can be reconfigured to allow for TFET or MOSFET operation and can be tuned to be n-type or p-type. Owing to the proper choice of materials and careful engineering of device structures, record-high current densities have been achieved in 2D TFETs. Full-band atomistic quantum transport simulations of the fabricated devices agree quantitatively with the current−voltage measurements, which gives credibility to the promising simulation results of ultrascaled phosphorene TFETs. Using atomistic simulations, we project substantial improvements in the performance of the fabricated TFETs when channel thicknesses and oxide thicknesses are scaled down.**



KEYWORDS: *black phosphorus, TFET, reconfigurable, transistor, tunneling, low-power*

In recent years, two-dimensional (2D) semiconducting materials have attracted attention as channel material for next-generation transistors[1−10] because the ultrathin body allows for ideal electrostatic control of the channel potential, addressing problems in conventional devices related to channel length scaling.[11,12] However, regardless of the actual channel material, in conventional MOSFETs, the current flowing below threshold is always determined by thermionic emission over the gate controlled barrier between source and drain, which fundamentally limits the subthreshold swing (SS) to about 60 mV/dec at room temperature. Among other things, this hinders scaling down the supply voltage and prevents further, urgently needed, reduction in power dissipation. Therefore, apart from new materials for transistor applications in general, novel devices based on alternative switching mechanisms are required to break the thermal limit and to achieve ultra-low-power device operation. Band-to-band tunneling (BTBT) field-effect transistors (TFETs)[13−20] have been proposed and demonstrated as promising candidates for achieving steep-slope devices. Combining this concept with using 2D materials as the active channel in TFETs allows benefiting from the ultrathin body thickness aspect of 2D, which leads to short tunneling distances. Small tunneling distances in turn result in both high "on"-state currents (I_{ON}) and steep SS values.[20−24]

Various research articles on building TFETs using 2D materials have been published over the last years. Most of this work focused on 2D vertical heterojunctions, such as molybdenum disulfide (MoS_2)/tungsten diselenide (WSe_2),[18] tin diselenide ($SnSe_2$)/BP,[25] and $SnSe_2$/WSe_2.[26] Some[22,27,28]

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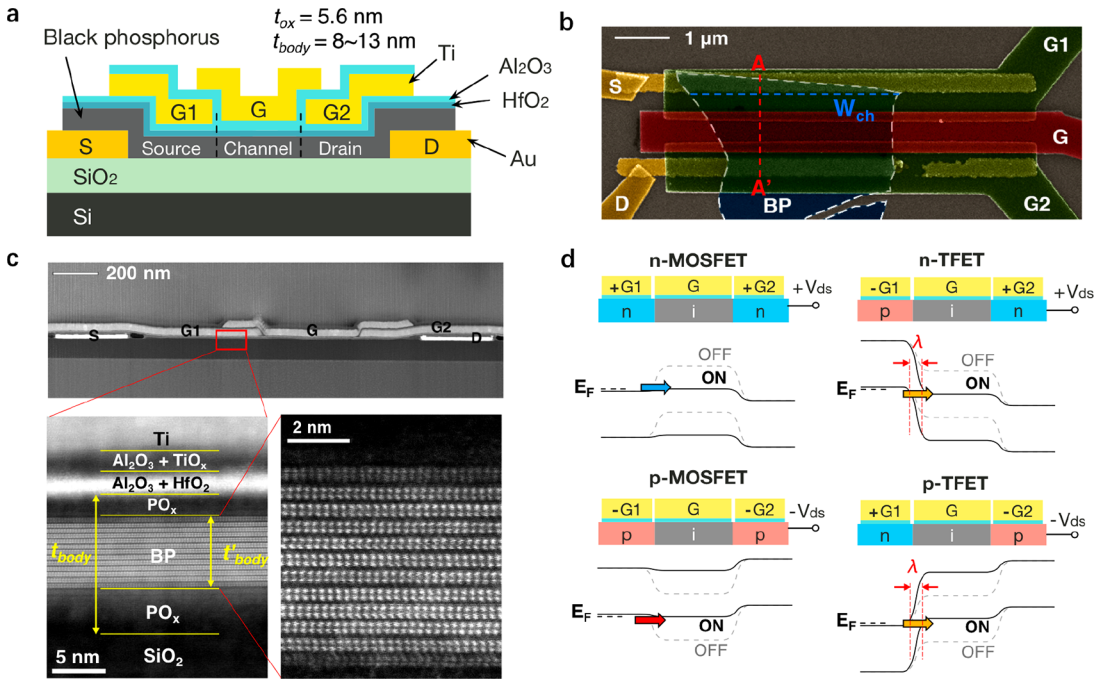

Figure 1. Black phosphorus RED-TFET. (a) Schematic of the BP RED-TFET. (b) Representative false-colored SEM image of the BP RED-TFET. Scale bar: 1 μm. (c) Representative cross-section HAADF-STEM image of the BP RED-TFET along A−A′ in panel b, showing the triple top-gate structure, the interface of BP and gate oxide, and the crystal structure of BP. Notice that due to oxide formation on both sides of BP, the real body thickness t'_{body} is smaller than the nominal body thickness t_{body}. (d) Schematic illustration of the bands through the BP channel when reconfiguring the RED-TFET in the four operation modes, enabled by electrostatic doping as controlled by V_{g1} and V_{g2}.

studied homojunction TFETs based on WSe_2, a 2D material intensively evaluated for TFET applications.[22,23] However, all of these tunneling devices suffer from low current levels. To evaluate the "on"-current I_{ON} for TFETs, it is instructive to take a look at the transmission probability, T, that describes charge transport through the BTBT barrier, based on the Wentzel−Kramer−Brillouin (WKB) approximation:[29,30]

$$T_{WKB} = \exp\left(-\frac{4\lambda\sqrt{2m^*E_g^3}}{3\hbar(\Delta\Phi + E_g)}\right) \quad (1)$$

where E_g is the bandgap; m^* is the tunneling effective mass; $\lambda = \sqrt{(\epsilon_{body}/\epsilon_{ox})t_{ox}t_{body}}$ is the screening length, which describes the spatial extent of the tunneling junction, in which t_{ox} and t_{body} are oxide thickness and body thickness, respectively; ϵ_{ox} and ϵ_{body} are dielectric constants of oxide and body, respectively; and $\Delta\Phi$ is the energy window of BTBT, *i.e.*, the energy difference between the conduction band edge in the n-type region and the valence band edge in the p-type region. To achieve a high transmission probability, E_g and m^* need to be minimized by choosing a suitable material, and λ needs to be reduced by improving the electrostatics in the device. TFETs built from WSe_2 exhibit thus unavoidably low I_{ON} values because the large band gap[31] (1.0 to 1.5 eV) and high effective masses[22] (electron effective mass $m_e^* = 0.34\ m_0$, hole effective mass $m_h^* = 0.44\ m_0$) of WSe_2 give rise to a low transmission probability. However, black phosphorus (BP) as channel material[8−10,32−36] is characterized by a tunable small bandgap[10,37,38] (0.3 to 2 eV) and low effective mass[37] (0.15 m_0) and can thus be expected to be a better material choice for high "on"-current TFET applications.[20,39,40] Based on few-layer BP, here we report experimental results on complementary lateral TFET, with BTB tunneling occurring at electrostatically[27,41,42] defined p/n (or n/p) homojunctions that can be controlled by means of multiple gates. We call this device a reconfigurable electrostatically doped tunneling field-effect transistor (BP RED-TFET). It is worth noticing that such electrostatically doped TFETs based on BP and reconfigurable operations have been demonstrated before.[40] In this article, we report both n-type and p-type operations in BP TFETs for the first time. In addition, we demonstrate record-high current drive densities and improved room-temperature subthreshold slopes through an optimized device structure.

RESULTS

Device Structure and Operation Principle. Figure 1a,b shows the schematic and a scanning electron microscopy (SEM) image (false-colored for clarity) of a BP RED-TFET. A few-layer BP flake is located on top of Au source/drain contacts, and two top-gates overlapping with the source and drain electrodes, G1 and G2, can be used to induce the desired electrostatic doping in the source and drain portions (next to the contact electrodes) of the BP, while the middle top-gate G controls the channel region. The silicon back-gate is kept floating in all measurements. Devices employed in this study have varying flake thicknesses as measured by AFM between 8 and 13 nm. Figure 1c shows a representational cross-section high-angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) image of the BP RED-TFET cross-section cut along the A−A′ line depicted in Figure 1b. The triple-gate structure of the device is clearly visible in the low-magnification image; the high-magnification details (images below) show the interface of BP with the gate oxide and the crystalline structure of BP. Note that there are amorphous-like layers both on the top and on the bottom of the BP layer, presumably PO_x (see Supplementary Figure S1d−g). These unexpected layers not only reduce the

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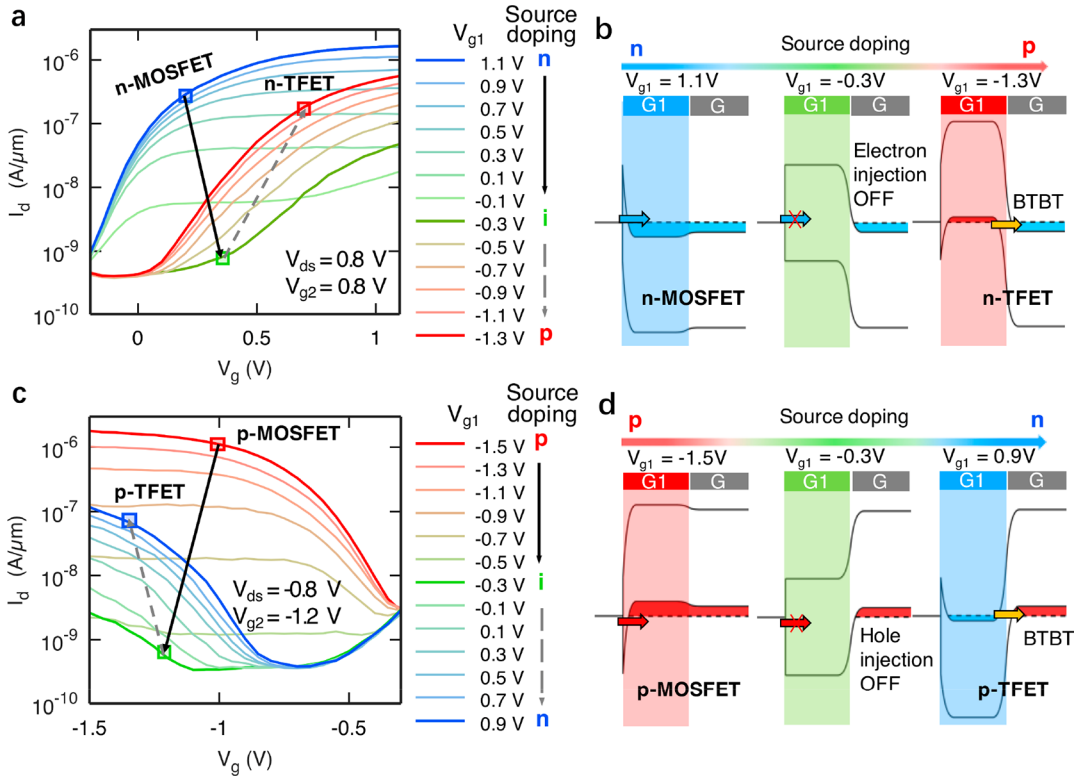

Figure 2. Transfer characteristics and reconfiguration of the BP RED-TFET. (a, c) Transfer characteristics of the BP RED-TFET in (a) n-type and (c) p-type configurations under different source doping conditions, showing the transition from the MOSFET mode to the TFET mode. (b, d) Band diagrams of the RED-TFET in (b) n-type and (d) p-type configurations corresponding to different source doping conditions in panels a and c, respectively.

thickness of the active BP layer as discussed in the simulation section but also change the actual electrostatics and gate dielectric film thicknesses (see Supplementary Section 1). Owing to the electrostatic doping approach implemented here, the doping profile along the source/channel/drain regions is electrically tunable, as shown in Figure 1d, which enables the reconfiguring of the device to different operation modes: (1) n-type TFET with a p/i/n profile, (2) n-type MOSFET with an n/i/n profile, (3) p-type TFET with an n/i/p profile, and (4) p-type MOSFET with a p/i/p profile.

Depending on the operation mode, the device is characterized by different carrier injection mechanisms. As shown in Figure 1d, in the n-type (or p-type) MOSFET mode, by applying a positive (or negative) gate bias V_G to the middle gate G, the bands in the "i" channel region are moved downward (or upward) to allow electrons (or holes) to be thermally injected from the source into the channel, turning the device from "off" to "on". However, in the n-type (or p-type) TFET mode, applying a positive (or negative) V_G opens up a band-to-band tunneling window at the source-to-channel junction (Figure 1d), turning the device from "off" to "on".

Similar triple-gate structures and reconfigurable operation have been reported in other articles.[27,40,41] However, not all four operation modes were achieved in these devices, and the reported current drive in the TFET mode is relatively small. In our devices, we have in particular optimized the contacts to enable both electron and hole injection, which allows us to access all four possible operation modes. The key lies in utilizing the top gates G1 and G2 to include gating of BP in the source and drain contact regions. Note that our BP films are located on top of the source and drain contact. We have also carefully engineered the gate structure to reduce oxide thickness and spacer thickness between the gates. Therefore, in the TFET modes, the thin gate dielectric thickness (t_{ox}) and a thin body thickness (t_{body}) together enable ideal electrostatics and ensure the abruptness of the tunneling junction through a small λ value, enabling us to achieve the lowest room-temperature SS and highest I_{ON} at V_{ds} = 0.8 V to date in 2D homojunction TFETs.

Electrical Characterization. Figure 2a shows the transfer ($I_d - V_g$) characteristics of a BP RED-TFET as a function of V_{g1} in n-type configuration, *i.e.*, for positive V_{ds} and V_{g2} (V_{ds} = 0.8 V, V_{g2} = 0.8 V). To illustrate the reconfigurability of our devices, first, a positive bias is applied to G1 (V_{g1} = 1.1 V), resulting in an effective n-doping of both the source and the drain region; the device thus exhibits an n/i/n doping profile across the BP flake and operates in the n-type MOSFET mode. When V_{g1} decreases progressively until V_{g1} = −0.3 V, the n-doping level in the source region becomes lower and electron injection from the source metal contact into the source region is gradually suppressed, as shown in the band diagram in Figure 2b, resulting in steadily decreasing current levels as indicated by the solid black arrow in Figure 2a.

Next, when the G1 voltage is further decreased beyond V_{g1} = −0.3 V, the doping in the source region becomes p-type. Under these conditions, current levels start increasing again, indicated by the dashed gray arrow in Figure 2a. This, at first glance, surprising non-monotonic trend occurs because when the source doping is made effectively p-type, the device changes from a conventional n-type MOSFET with an n/i/n doping profile to an n-type TFET with a p/i/n doping profile and a BTBT window at the source-to-channel junction is opened, as shown in Figure 2b. As V_{g1} is further decreased, the source

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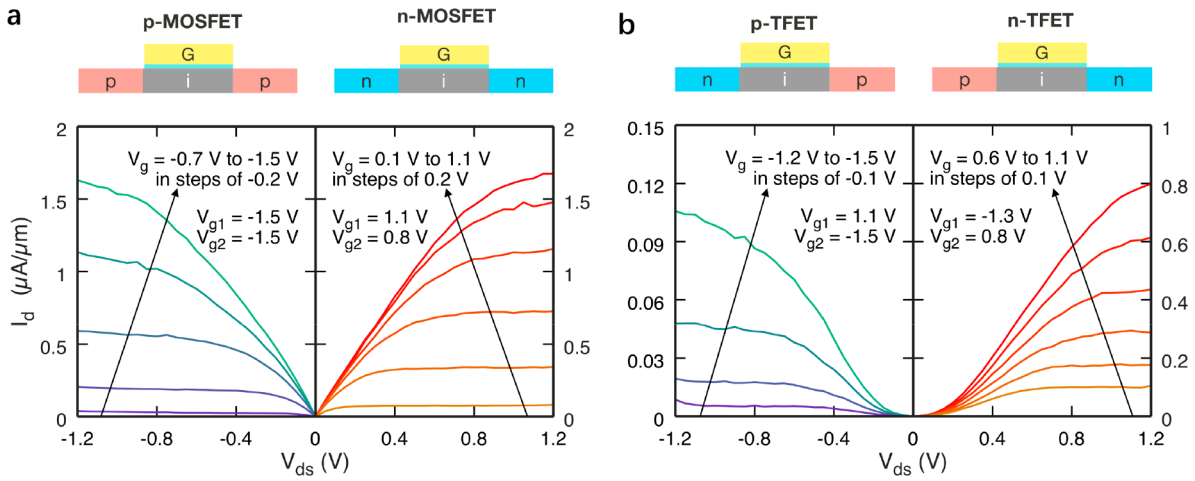

Figure 3. Output characteristics of the BP RED-TFET. (a) Output characteristics of the BP RED-TFET in the p-type and n-type MOSFET mode. The saturation behavior indicates a good gate control on the channel. (b) Output characteristics of the BP RED-TFET in the p-type and n-type TFET mode. Nonlinear output onsets are observed due to the drain-induced-barrier thinning (DIBT) effect.

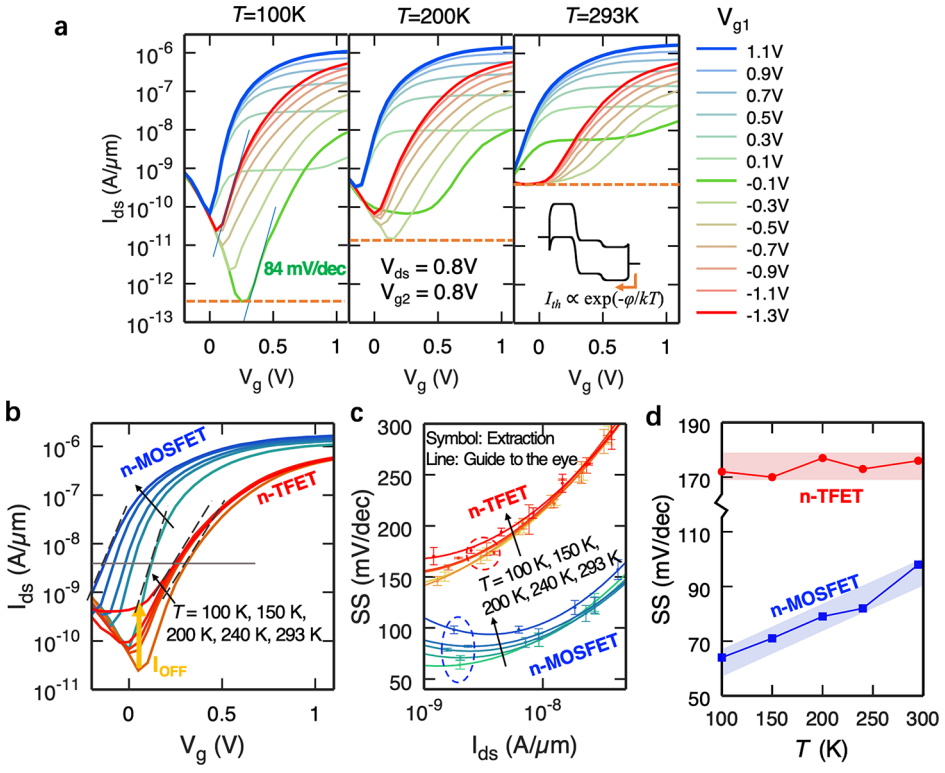

Figure 4. Temperature-dependent measurements. (a) Comparison of transfer characteristics of the BP RED-TFET at 100, 200, and 293 K, showing increasing off-current levels at elevated temperatures. Dashed orange lines indicate thermionic current and trap-assisted current cutoff limits. The inset shows a band diagram explaining the impact of thermionic injection from the drain at higher temperatures. (b) Comparison of transfer characteristics of the BP RED-TFET in the n-type MOSFET mode and the n-type TFET mode at different temperatures. In the n-TFET mode, the transfer characteristics show a weaker temperature dependence compared to the operation in the n-MOSFET mode except for a rise in the minimum off current level due to thermal injection. (c) Comparison of experimental subthreshold swing (SS) values *vs* drain current I_d in the n-type MOSFET mode and the n-type TFET mode at different temperatures. In the n-TFET mode, SS shows weaker temperature dependence. (d) Comparison of experimental SS values *vs* temperature for the BP RED-TFET operating in the n-type MOSFET mode and the n-type TFET mode.

region becomes even more substantially p-doped, and the BTBT window is enlarged, resulting in further increased current levels, as illustrated by the dashed gray arrow in Figure 2a. This non-monotonic trend of current level change with V_{g1} or, equivalently, source doping level is unambiguous evidence for our claim of BTB tunneling in the device. Moreover, the reconfigurable operation of our BP RED-TFET from the MOSFET mode to the TFET mode by tuning the source doping is demonstrated in this way.

Similarly, transfer characteristics of a BP RED-TFET as a function of V_{g1} in p-type configuration, *i.e.*, for negative V_{ds} and V_{g2} (V_{ds} = −0.8 V, V_{g2} = −1.2 V) are shown in Figure 2c. When

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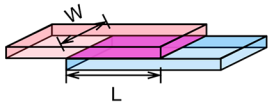
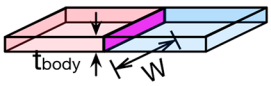
ACS Nano 2019, 13, 377−385

Table 1. Comparison of 2D TFETs[a]

Structure	Ref.	Material	I_{ON}	Area	Current density	Minimum SS @300K	ON/OFF	Reconfigurable
Vertical heterojunction 	[18]	MoS_2/WSe_2	5 nA (V_{DS}=-1.5 V)	~2 μm×4 μm	0.06 A/cm^2	130 mV/dec	10^4	Yes
	[25]	BP/$SnSe_2$	10 μA (V_{DS}=-1 V)	~9 μm×8 μm	13 A/cm^2	--[1]	--[1]	No
	[26]	WSe_2/$SnSe_2$	4 μA (V_{DS}=-1 V)	~140 μm^2	3 A/cm^2	164 mV/dec	10^6	Yes
Lateral homojunction 	[27]	WSe_2	1.2 nA/μm (V_{DS}=-0.5 V)	3 nm×1 μm	40 A/cm^2	366 mV/dec	10^2	Yes
	[40]	BP	0.2 μA/μm (V_{DS}=-2 V)	~5 nm×1 μm	4×10^3 A/cm^2	595 mV/dec	10^2	Yes
	Our work	**BP**	**0.6 μA/μm (V_{DS}=0.8 V)**	**3 nm×1 μm**	**2×10^4 A/cm^2**	**170 mV/dec**	**10^3**	**Yes**

[1] Tunneling diode

[a]The tunneling area is defined by $W \times L$ in a vertical heterojunction, and $W \times t_{body}$ in a lateral homojunction, where W and L are channel width and channel length, respectively. Because the tunneling area is independent of L in a lateral homojunction, this device layout exhibits better scaling potential.

the source doping is changed from p-type to n-type by sweeping the G1 bias from $V_{g1} = -1.5$ V to $V_{g1} = 0.9$ V, one observes a similar nonmonotonic trend of current level change as in Figure 2a and reconfiguration from the p-type MOSFET mode to the p-type TFET mode. The band diagrams of our BP RED-TFET changing from the p-type MOSFET mode to the p-type TFET mode are shown in Figure 2d.

The output characteristics ($I_d - V_{ds}$) of the BP RED-TFET configured in (a) the p-type and n-type MOSFET mode and (b) the p-type and n-type TFET mode are displayed in Figure 3. Output saturation is observed for all four operation modes, indicating a good electrostatic control of the channel by the gate. Note that in the TFET modes, I_d increases nonlinearly with V_{ds} for small V_{ds} values (Figure 3b). While nonlinear output characteristics are often seen as a sign for Schottky-barrier contacts, this explanation does not apply in our case. In fact, if the nonlinearity would indeed be caused by the contacts, the device operating in the MOSFET modes with the same source doping configurations would also exhibit nonlinearity in the output characteristics, which is clearly not the case in Figure 3a. Instead, the observed nonlinear increase in I_d originates from drain-induced-barrier-thinning (DIBT) of the BTBT barrier,[16] which is a consequence of the relatively large quantum capacitance of the black phosphorus channel. Therefore, it is exclusive to TFETs and not observed in MOSFETs where BTB tunneling barriers are absent. Note that in a 1D carbon nanotube device with low quantum capacitance, DIBT can be suppressed in the quantum capacitance limit,[43] and linear output characteristics can be recovered.[16]

Temperature-Dependent Measurement. Transfer characteristics of the BP RED-TFET in n-type configuration at different temperatures are shown in Figure 4a. It is apparent that lowering the temperature results in reduced "off"-current levels due to suppressed thermionic injection from the drain (see inset of Figure 4a) and suppressed trap-assisted transport.[40] Figure 4b shows a comparison of temperature-dependent $I_d - V_g$ characteristics for a device operating in the n-type MOSFET mode and in the n-type TFET mode. The device shows distinctly different temperature dependences when operating in these two modes due to different injection mechanisms. In the MOSFET mode, the carriers are thermally injected into the channel; therefore, $I_d - V_g$ has a strong dependence on temperature. In contrast, the carrier injection mechanism is BTB tunneling in the TFET mode, and $I_d - V_g$ displays a much-weaker dependence on temperature,[13] as shown in Figure 4b. Note that the increasing minimum "off" current with temperature in the case of the TFET is due to an increase in thermionic injection at higher temperatures over the drain barrier biased at positive V_{g2} values. Figure 4c shows SS values *versus* drain current I_d in the n-type MOSFET mode and the n-type TFET mode at different temperatures, where the latter clearly shows a weaker temperature dependence. Figure 4d compares SS values *versus* temperature for the same device operating in the MOSFET mode and in the TFET mode. SS values are extracted near a constant current of 5 nA (as shown in circles in Figure 4c) to avoid the impact of the temperature-dependent thermionic current cutoff (dashed orange lines in Figure 4a) on the SS extraction. As expected, SS values increase with temperature in case of the MOSFET mode while remaining constant in the TFET mode.

Also note that the minimum SS value at room temperature for band-to-band tunneling is 178 mV/dec, well above 60 mV/dec This is, in part, due to the choices of flake thickness and gate dielectrics as discussed below but also related to the fact that the steepest slopes in case of TFETs occur at the lowest current levels. In fact, when analyzing the green curve at $V_{g1} = -0.1$ V at 100 K, a minimum SS value of 84 mV/dec is extracted.

DISCUSSION

Previous studies on building TFETs using 2D materials[18,25,26] mainly focused on vertical heterostructures. This is in part due to the difficulty in achieving chemical doping in 2D materials[44] (which is resolved here using electrostatic doping), while in heterostructures, the band alignment between different 2D materials can be leveraged to construct a tunneling p−n junction. Lateral homojunction TFETs, which are the focus of this study and prior work,[40] have better scaling potential compared with vertical heterojunction TFETs. In this context, Figure S7 shows a comparison of the area scaling of a vertical and a lateral TFET. Because the tunneling area in a vertical TFET is

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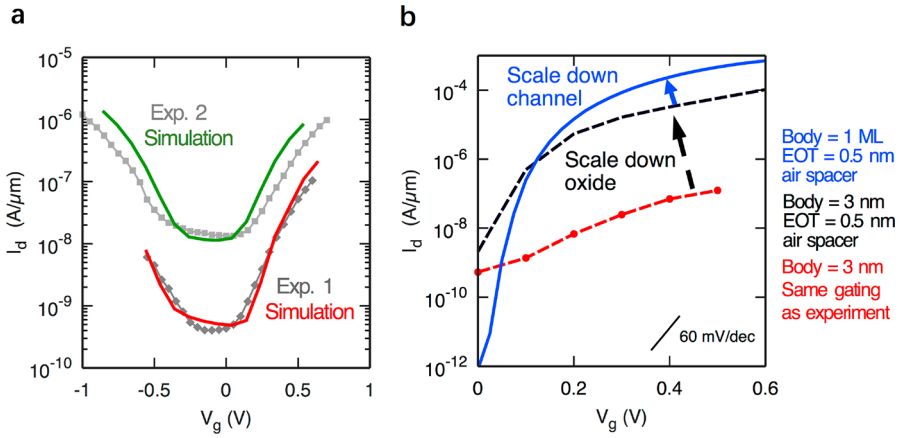

Figure 5. Projections for BP TFET performance. (a) Atomistic simulations, solid lines, of $I_d - V_g$ for two exemplary BP TFETs, showing good agreement with experimental data (gray dots). "Exp. 1" refers to measurements performed on a device as shown in Figure 1 with a nominal 8.3 nm body and with gate G1 and G2 having configurations (−1.3 and 0.8 V). The simulation has been performed with a smaller BP thickness of 3 nm and a thicker oxide to account for the oxidation (see Supplementary Section 1). "Exp. 2" is a measurement of an earlier prototype device with a thicker BP flake of 12.8 nm that has been simulated with 7 nm to account for the oxidation. (b) Simulation of the fabricated BP TFET shown in red. Improving the electrostatics by using HfO_2 with an EOT of 0.5 nm is expected to significantly improve steepness and current levels, as shown in blue. Further improvements can be achieved by scaling down the channel into a monolayer (ML) BP and incorporating air spacer, as shown in black. Notice that due to the larger bandgap of ML BP, the current levels are lower without proper electrostatics enabled by an air spacer, as shown by the gray dashed line.

proportional to the channel length L, the normalized "on" current will decrease proportionally when scaling down the channel length, as shown in Figure S7a. Moreover, the accessible steep slope regime of the subthreshold characteristics will also decrease after scaling. This means achieving steep slopes alone, without high "on" currents, is of little practical value. However, lateral TFETs do not suffer from the same scaling dilemma.

Table 1 shows a comparison of 2D TFETs from previous publications and our work. As evident, BP TEFTs as discussed here are achieving the highest tunneling current densities, *i.e.*, 2×10^4 A/cm^2, a critical step in the development of TFETs. From the table, one can readily see that all vertical TFETs exhibit rather-low tunneling current densities of ∼10 A/cm^2, 3 orders of magnitude lower than reported here, which is compensated by employing a large tunneling area of ∼10 μm × 10 μm in the prototype device demonstrations. Scaling down the channel length into the submicron regime, the "on" current will drop by orders of magnitude and become too low for practical applications. While previous vertical heterojunction 2D TFETs are important proof-of-concept demonstrations for steep-slope devices, they fundamentally lack the scaling potential as required for modern integrated circuits (ICs).

In contrast, the "on" current of a lateral device will not be affected by channel length scaling, as shown in Figure S7b, which means that lateral TFETs are more-promising candidates for scaled devices than vertical TFETs.

To boost the performance of BP TFETs further, channel body and oxide thicknesses need to be aggressively scaled down.[23] As one can see from eq 1, the performance of a TFET not only depends on material parameters such as E_g and m^* but also, in particular, on the screening length λ, which, in turn, depends on t_{ox} and t_{body}. To make quantitative projections about the potential performance improvement of 2D BP TFETs with scaled-down t_{ox} and t_{body}, self-consistent atomistic simulations are first performed using the NEMO5 toolsets[45,46] to match the experimental data obtained in this study. Figure 5a shows a comparison of simulated $I_d - V_g$ and measured TFET characteristics, showing good agreement between simulation and experimental data. Note that to achieve this matching we made use of our findings from Figure 1c. To describe the experimental results (Exp. 1) for a device with a nominal thickness of t_{body} = 8.3 nm and t_{ox} = 5.6 nm properly, t'_{body} = 3 nm and t'_{ox} = 7.5 nm were assumed in the simulations to account for formation of the above-mentioned PO_x layers, where t'_{body} and t'_{ox} denotes the real body thickness and real oxide thickness, respectively, after considering the formation of PO_x layers (see Supplementary Section 1). Under these assumptions, both, the inverse subthreshold slope as well as the actual current levels are properly reproduced (see Figure 5a). Moreover, when performing a similar comparison for a device from a slightly thicker BP flake, a t'_{body} of 7 nm and a t'_{ox} of 8.1 nm in the simulation nicely match the experimental results for the nominal values of t_{body} = 12.8 nm and a t_{ox} = 6.2 nm (Exp. 2 in Figure 5a; see Supplementary Section 8). All simulations are performed with transport direction along the armchair direction of BP (see Supplementary Section 6). With this calibration in place, we are in a position to carry out projections based on simulations for aggressively scaled BP TFETs. Figure 5b shows the simulated $I_d - V_g$ of a BP TFET when scaling down the oxide to an equivalent oxide thickness (EOT) of 0.5 nm while keeping the same channel thickness of t'_{body} = 3 nm (blue line). This approach results in significant improvements in the steepness of the subthreshold region and "on"-current levels. Moreover, further scaling down the channel thickness to a single monolayer (black line) and etching the spacers between separate gates to achieve better electrostatic conditions[47] result in I_{ON} values of 800 μA/μm and SS values of 12 mV/dec, clearly highlighting the potential of BP TFETs in future applications. It is worth noticing that monolayer BP exhibits a much-larger bandgap than few-layer[10,37] (∼2 eV compared to ∼0.3 eV); therefore, scaling down the channel thickness to a single monolayer without introducing an air spacer results in a lower current level (gray dashed line), and the employment of the novel air-spacer structure amplifies the electric field in the tunnel junction,[47] compensating for the increase in bandgap and, as a result, boosting the "on" current to 800 μA/μm (black line).

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ACS Nano 2019, 13, 377−385

CONCLUSIONS

In conclusion, we have demonstrated reconfigurable complementary BP TFETs. The TFETs exhibit "on"-currents of up to 0.6 μA/μm and sub-threshold swings of 170 mV/dec at room temperature for V_{ds} = 0.8 V in n-type configuration and "on"-currents of up to 0.14 μA/μm and sub-threshold swings of 174 mV/dec at room temperature for V_{ds} = −0.8 V in p-type configuration. Record-high tunneling-current densities of 2×10^4 A/cm^2 have been achieved in the TFETs through proper choice of material and optimization of device structure. Our devices can be reconfigured to behave as an n/p-type TFET and as an n/p-type MOSFET owing to the electrostatic doping control of three separate top gates. Atomistic simulations predict that the performance of BP TFETs can be further improved toward I_{ON} = 800 μA/μm and SS = 12 mV/dec with scaled down channel and oxide thicknesses. Our BP RED-TFET provides a guide for energy-efficient tunneling devices based on 2D materials.

METHODS

Device Fabrication and Electrical Characterization. Ti/Au (10 nm/20 nm) contacts were deposited onto a silicon substrate with 90 nm of silicon dioxide (SiO_2) on top and patterned using e-beam lithography and a lift-off process. BP flakes were exfoliated onto the Au contacts from bulk crystals, purchased from Smart Elements (purity 99.998%), using mechanical exfoliation with standard dicing tape purchased from Semiconductor Equipment Corp. The exfoliation is performed in ambient atmosphere; however, care was taken to minimize the time that BP flakes were exposed to the air (less than 30 min). A thin layer of Al was e-beam-evaporated on top of BP, which formed a 1.3 nm thick aluminum oxide upon exposure to air and acted as seeding layer for the subsequent ALD process. A bilayer dielectric stack composed of 0.8 nm of HfO_2 and 2.2 nm of Al_2O_3 was deposited by a thermal ALD process at 200 °C to form gate dielectrics for G1 and G2. Next, G1 and G2 were defined by subsequent e-beam lithography and e-beam evaporation of 40 nm Ti. The sample is annealed in forming gas for 3 h at 300 °C to improve the quality of the gate dielectric. To achieve proper isolation between gates G1/G2 and G while maintaining relatively thin dielectric thicknesses for gate G, the Al_2O_3 between the G1 and G2 regions was removed by wet etching, with G1 and G2 metals as masks and HfO_2 as etch stop layer. A second ALD process was performed to deposit another 3.5 nm Al_2O_3 layer as gate dielectric for G as well as to ensure isolation between G1/G2 and G. The total oxide thickness for gate G is 5.6 nm. The device fabrication is finalized by depositing 40 nm Ti to form gate G. Room-temperature and low-temperature electrical characterization of the device was performed in a LakeShore FWPX Cryogenic Probe Station at a vacuum level below 10^{-5} Torr using an Agilent 4156C parameter analyzer.

Atomistic Simulation. The atomistic quantum transport simulation results have been obtained from a self-consistent solution of the 3D Poisson equation and by employing the non-equilibrium Green's functions (NEGF) method using the Nanoelectronics modeling tool NEMO5.[45,46] The Poisson equation provides the potential for the NEGF method and takes the free charge in return. The tight-binding Hamiltonian of phosphorene used in NEGF calculations employs a 10-band sp3d5s* second-nearest neighbor model. More details on the Poisson equation with anisotropic dielectric tensor and NEGF equations can be found in our previous works.[20,21]

Transmission Electron Microscopy Characterization. An FEI Nova NanoLab 600 DualBeam (SEM/FIB) was employed to prepare cross-sectional TEM samples. Carbon was deposited on top of the device to protect the surface. To reduce Ga ion damage, in the final step of preparation the TEM samples were thinned with 2 kV Ga ions using a low beam current of 29 pA and a zero-degree incident angle. An FEI Titan 80−300 probe-corrected scanning transmission electron microscope (STEM) equipped with monochromator and GIF Tridiem electron energy loss spectrometer (EELS) system was employed to acquire atomic-resolution high-angle annular dark field (HAADF) images and EELS-based spectrum images. HAADF images were acquired with the detector semiangular collection range of 35−195 mrad. The spectrum-images were acquired with a condenser aperture convergence semiangle of 13 mrad and a spectrometer entrance aperture collection semi-angle of 14 mrad.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b06441.

Additional details and figures on the thickness determination of BP, drain doping impact on the ambipolar branch, hysteresis in transfer characteristics, gate leakage current, stability of BP, effects of BP orientation and transport direction on BTBT, scaling of vertical and lateral TFETs, device structure, and characteristics of an earlier prototype device (PDF)

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P.W. and J.A. conceived of the idea and designed the experiment. P.W. performed the device fabrication, electrical characterization, SEM imaging. and AFM measurement. T.A. performed the atomistic simulations. T.A., H.I., G.K., and R.R. developed the simulation framework and analyzed the simulation. H.Z. prepared TEM samples using SEM and FIB and conducted TEM and STEM imaging. H.Z., L.A.B., and A.V.D. did TEM and STEM data analysis. P.W. and J.A. wrote the manuscript with input from T.A. All authors discussed the results and commented on the manuscript. J.A. supervised the project.

Notes

The authors declare no competing financial interest.

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Supplementary Information for

Complementary Black Phosphorus Tunneling Field-Effect Transistors

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1. Thickness determination of BP

It is well known that BP readily oxidizes and forms PO_x upon exposure to air by reacting with oxygen and water.[1,2,3] In addition to air exposure during the device fabrication process, the BP surface was also exposed to a water rich environment at elevated temperatures (200 °C) during the ALD gate oxide deposition. Since the electrically active BP layer thickness is a critical parameter for the tunneling currents in our devices, it is important to determine the thicknesses of the oxidized layers and the thickness of the remaining crystalline BP layer in the total BP flake thickness.

Figure S1(a) shows an AFM image and line scan of a t_{body}=8.3 nm thick BP flake as the active channel in one of the BP RED-TFETs with a nominal t_{ox}=5.6 nm thick Al_2O_3/HfO_2 gate dielectric stack as described in the manuscript. Figure S1(b) shows a comparison of the experimentally measured I_d-V_g curve of this device and a set of simulations with different flake thicknesses. In our simulations, we have considered both the reduction of the body thickness and the increase of the oxide thickness as a result of oxidation, and we assume the resulting PO_x layers on the top and on the bottom side of BP are of the same thickness (note that only the PO_x layer on the top contributes to the gate dielectric thickness t'_{ox}). The dielectric constants of the oxides used in the simulation are 8 for Al_2O_3, 16 for HfO_2 and 5.4 for PO_x. The chemical composition of the PO_x layer formed on black phosphorus is assumed to be P_2O_5 (ref. 3) and the dielectric constant is estimated from phosphate glass,[4] in which P_2O_5 acts as glass former. As apparent from Figure S1(b), a body thickness of t'_{body}=3 nm and a t'_{ox}=8.3 nm (t_{ox}=5.6 nm, plus additional 2.7 nm of PO_x layer) results in the best match between experiment and simulation.

To verify our assumption of a substantial reduction in BP body thickness and corresponding increase of dielectric layer thickness through the formation of PO_x, a careful TEM analysis on another BP RED-TFET that went through the same fabrication process was performed. The BP flake thickness in this device is determined to be t_{body}=12.8 nm from AFM measurements, as shown in Figure S1(c). Figure S1(d) shows an HAADF-STEM image of the BP RED-TFET. Figure S1(e) shows higher magnification HAADF-STEM images of the "G1-S" and "G1" regions, as depicted by the red and green boxes in Figure S1(d). The thicknesses of the BP crystalline layer and PO_x layers are labeled in the images, which are determined using the method described below.

Figure S1(f) shows an electron energy loss spectrum (EELS) in the "G1-S" region, which is the sum of all the background subtracted spectra acquired along the A-B line depicted in Figure S1(e), showing the P-*L*, O-*K* and Ti-*L* edges. Figure S1(g) shows the intensity profiles of the HAADF image (HAADFI) and EELS P-*L*, O-*K* and Ti-*L* edges along the A-B line in Figure S1(e). Combining the HAADF intensity profile and EELS line scan, one can determine the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1-S" region to be 1.4 nm and 6.9 nm respectively. The total flake thickness is 13 nm, which agrees reasonably well with the AFM measurement. Using the same method, we can measure the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1" region to be 1.9 nm and 6.7 nm respectively, with the total flake thickness being 12.2 nm. The discrepancy between the extraction in the G1-S and G1 region occurs reasonable considering the variations when preparing the sample for cross-section TEM and the uncertainty in determining the position of the interface between PO_x and SiO_2.

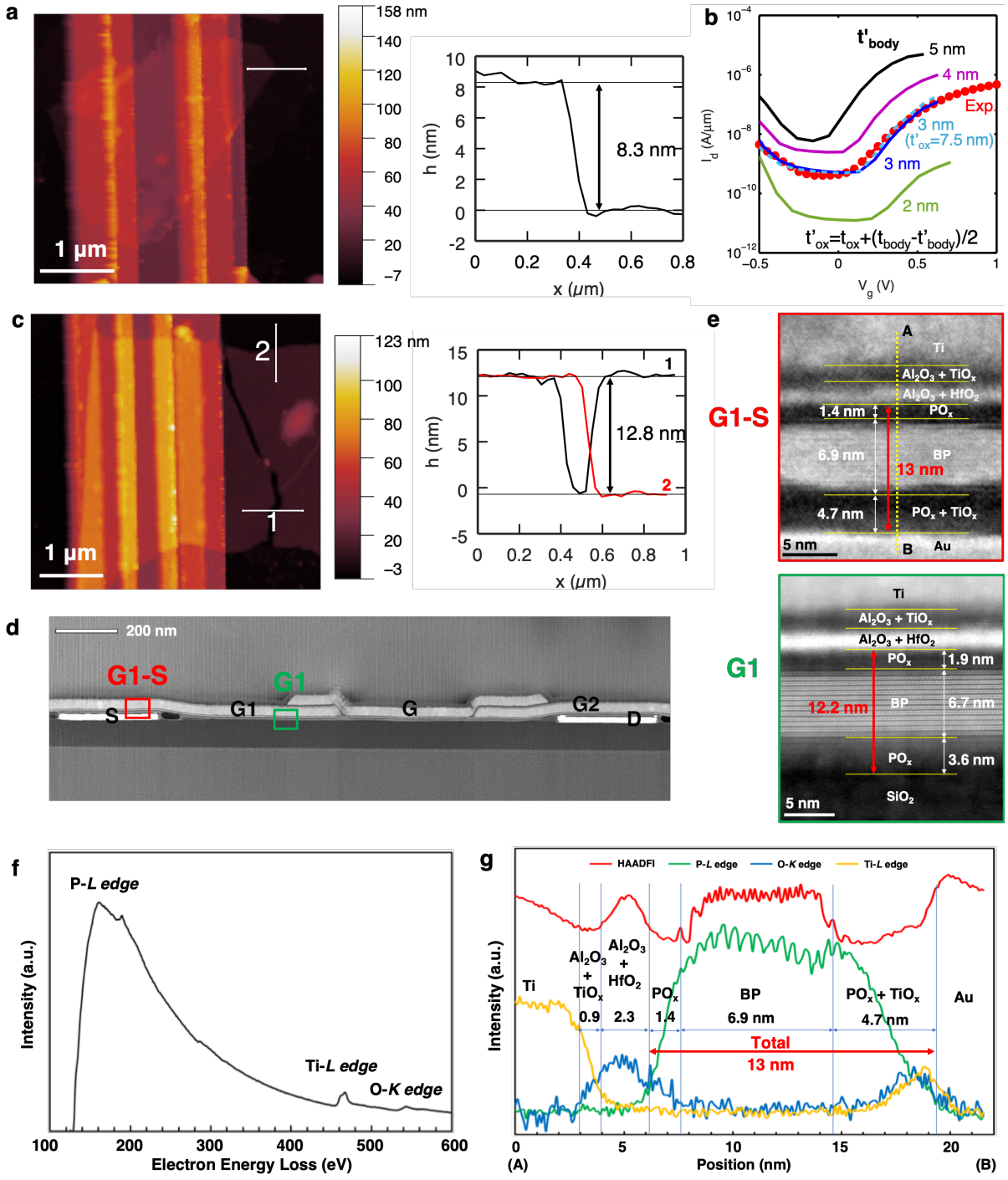

Figure S1. Thickness determination of BP. (a) AFM image and line scan of the BP flake used in the electrical characterization (t_{body}=8.3 nm). (b) Comparison of measured I_d-V_g curve of BP TFET (dots) and simulated I_d-V_g curves for different body thicknesses t'_{body} (lines). The simulation with t'_{body}=3 nm matches best with the experiment. (c) AFM image and line scan of the BP flake used in the TEM analysis (t_{body}=12.8 nm). (d) HAADF-STEM image showing the cross-section of the BP RED-TFET. (e) Higher magnification HAADF-STEM images from the regions defined by the red and green boxes in (d). (f) Background subtracted EELS spectra, showing the sum of all the spectra acquired along A-B line shown in (e). (g) Intensity profiles of HAADF image and EELS P-*L*, O-*K* and Ti-*L* edges along A-B line in (e), showing the thicknesses of crystalline BP and PO_x layers and total flake thickness.

In conclusion, from the TEM analysis, we have found that in a t_{body}=12.8 nm thick BP flake, the thickness of the BP crystalline layer is reduced to t'_{body}=6.9 nm. This means that in the t_{body}=8.3 nm thick BP flake, the BP crystalline layer thickness should be about t'_{body}=2.4 nm [~ 8.3 nm – (12.8 nm – 6.9 nm)]. Considering the uncertainty in the thickness measurements and device-to-device variations, t'_{body}=3 nm is a good approximation for the simulation framework employed in Figure S1(b). Note that to account for the thickness of the PO_x layer (~1.9 nm from the TEM analysis), the effective dielectric thickness of the Al_2O_3/HfO_2 plus PO_x gate dielectric stack is corrected to be t'_{ox}=7.5 nm (~ 5.6 nm + 1.9 nm) which is decomposed in the atomistic simulation into the various oxide layers.

2. Drain doping impact on ambipolar branch of the BP RED-TFET

Figure S2(a) shows the impact of drain doping on the ambipolar branch of the BP RED-TFET in n-type TFET mode. In the BP RED-TFET, the drain doping is achieved through electrostatic doping controlled by G2. Therefore, by tuning V_{g2} we can change the doping type and concentration in the drain region.

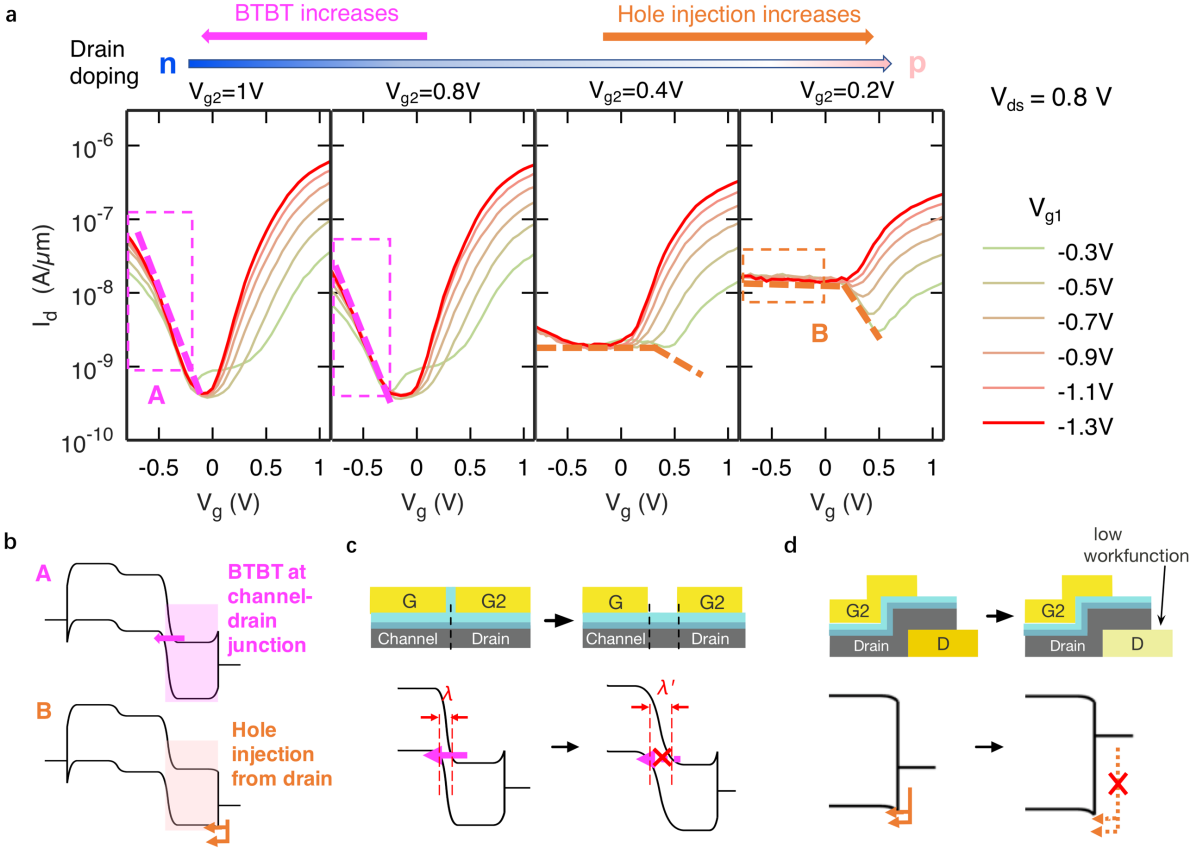

Figure S2. Drain doping impact on ambipolar branch of the BP RED-TFET. (a) Transfer characteristics of RED-TFET with different drain doping conditions, showing ambipolar currents due to two different carrier injection mechanisms. (b) Band diagrams for the two mechanisms of ambipolar currents: BTBT at the channel-drain junction and hole injection from drain. (c) Design for suppressing ambipolar BTBT by increasing tunneling distance at drain-channel junction. (d) Design for suppressing ambipolar drain injection by using a low workfunction drain contact.

First, when we apply V_{g2} = 1V, the drain is doped n-type, and when V_g is negative, there exists a BTBT tunneling path from the channel region to the drain, as is shown in the band diagram labeled with "A" in Figure S2(b). Therefore, in the transfer characteristics, we see an ambipolar branch corresponding to this BTBT current. When V_{g2} decreases to 0.8V, the n-doping in the drain region becomes weaker, and the ambipolar tunneling current becomes smaller, as can be seen from the transfer characteristics. However, if we further decrease V_{g2}, the drain doping decreases and eventually becomes p-doped, and the hole injection from the drain contact (both thermionic injection and tunneling through Schottky contact) becomes stronger, as is shown in the band diagram labeled with "B" in Figure S2(b). Therefore, both mechanisms A) ambipolar BTBT at the channel-to-drain junction and B) ambipolar hole injection from drain need to be addressed through proper choice of the drain doping to achieve the lowest possible OFF-current.

The ambipolar branch can be suppressed with an improved design of the RED-TFET. By introducing an underlap between the channel and drain regions,[5] or equivalently between G and G2 in the RED-TFET, the tunneling distance for BTBT between the channel and drain region is increased, as is shown in Figure S2(c), and therefore the ambipolar BTBT gets suppressed. The hole injection can be suppressed by increasing the Schottky-barrier height for hole injection at the drain, which can be achieved by using a low work function contact metal, as is shown in Figure S2(d).

3. Hysteresis in transfer characteristics of the BP RED-TFET

Figure S3 shows the transfer characteristics of a BP RED-TFET under two scan directions – solid line swept from 1.1 V to -0.6 V, and dashed line swept from -0.6 V to 1.1 V. The step in V_G is 0.05 V. In the electrical measurement, we set the integration time to "SHORT" when using the Agilent 4156C Parameter Analyzer and the scan rate is about 1 V/s. As can be seen from Figure S3, the hysteresis is less than 50mV, indicating a good-quality gate oxide has been formed on BP.

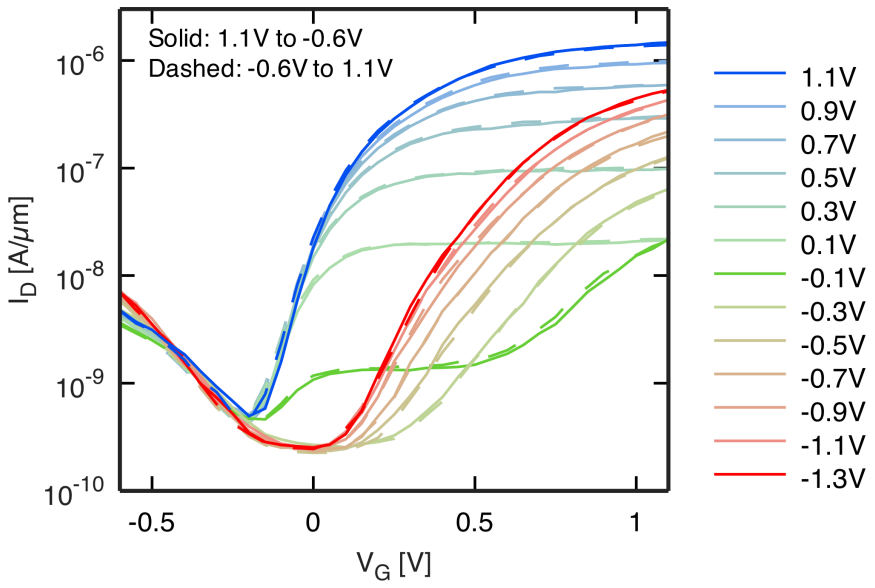

Figure S3. Hysteresis of transfer characteristics of the BP RED-TFET

4. Gate leakage current of the BP RED-TFET

Figure S4 shows the gate leakage currents of all three gates, G1, G2 and G, in the BP RED-TFET operating in MOSFET and TFET modes. All of the gate currents are more than one order-of-magnitude smaller than drain currents, which implies that the drain currents and SS extraction in this work are not impacted by gate leakage. Also note that most of the leakage currents result from leakage between gates (where $I_g = I_{g1}$ or $I_g = I_{g2}$), and the gate-to-channel leakage currents are accordingly even smaller.

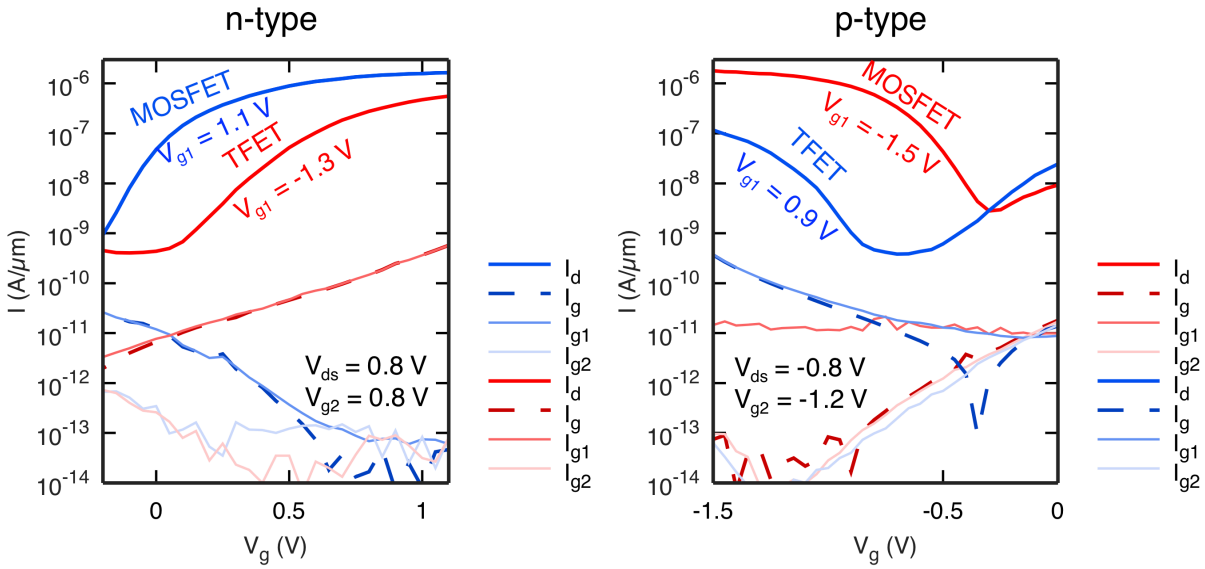

Figure S4. Gate leakage currents of the BP RED-TFET

5. Stability of black phosphorus

As mentioned in Section 1, BP readily oxidizes upon exposure to air, and the electrical properties of BP degrade with oxidation. Previous studies also show that the air stability of BP can be improved by means of passivation.[2,6,7] We found that the electrical properties of black phosphorus devices are rather stable if samples are stored in an inert environment or properly passivated.

Figure S5(a) shows the transfer characteristics of a BP RED-TFET measured immediately after fabrication and after storage in a nitrogen dry box for 4 months. The characteristics remain almost unchanged, except for a slight shift in threshold voltage.

We also studied the passivation of BP for achieving air-stable devices. 20 nm thick Al_2O_3 was grown on a BP FET using ALD to passivate the device. As is shown in Figure S5(b), the characteristics of the BP FET remain stable after storage in air over a time period of 180 days.

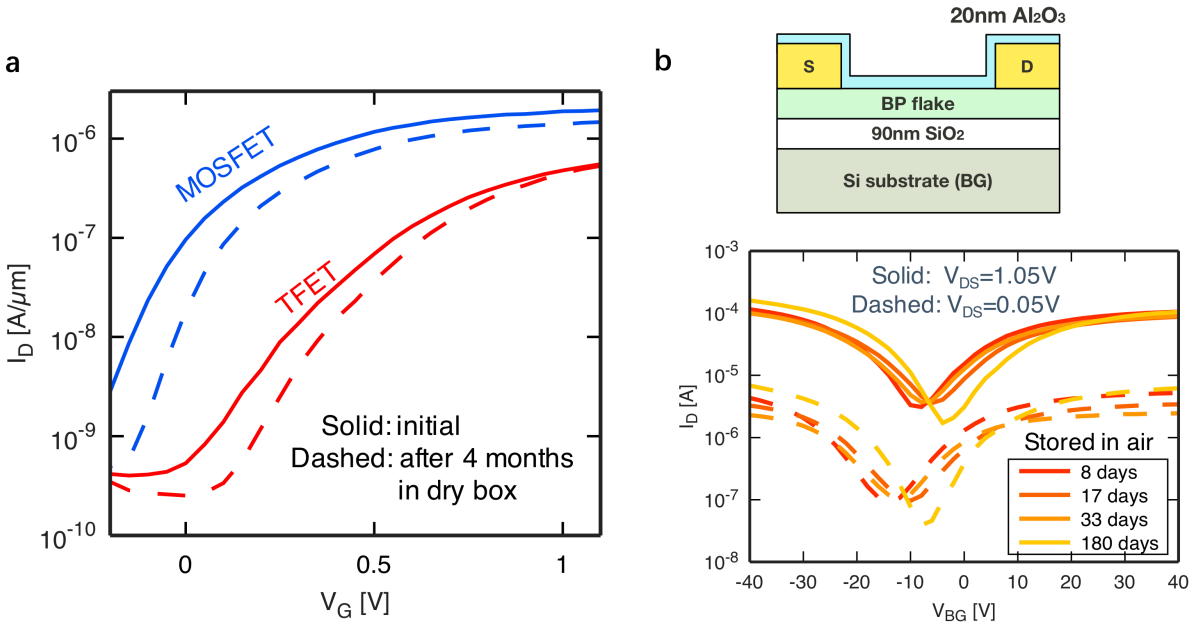

Figure S5. Stability of black phosphorus. (a) Comparison of transfer characteristics of the BP RED-TFET measured immediately after fabrication and after storage in an inert atmosphere for 4 months. No significant change is observed except for a shift in threshold voltage. (b) Transfer characteristics of a BP FET passivated by Al_2O_3. No significant changes are observed after storage in air for 180 days.

6. Effects of BP orientation and transport direction on BTBT

BP exhibits anisotropic effective masses along different transport directions.[8] DFT calculations[8] show that in monolayer BP, the carrier effective masses are 0.15 m_0 (holes) and 0.17 m_0 (electrons) in the armchair direction, and 6.35 m_0 (holes) and 1.12 m_0 (electrons) in the zigzag direction. On the other hand, in bulk BP, the values are 0.14 m_0 (holes) and 0.15 m_0 (electrons) in the armchair direction, and 0.71 m_0 (holes) and 1.15 m_0 (electrons) in the zigzag direction.

As we have discussed in the main text, the BTBT tunneling current is exponentially dependent on the effective mass. Therefore, the current level of a BP TFET depends on the transport direction. It has been experimentally demonstrated in ref [9] that the anisotropy of band-to-band tunneling in armchair direction and zigzag direction in BP can be up to 10^4. Here, we have investigated the effects of BP orientation on BTBT by both i) simulation and ii) a statistical study of experimental device currents.

Figure S6(a) shows the analytic modeling approach for the orientation-dependent BTBT current in BP TFETs. We have calculated a tunneling direction dependent transmission $T(\theta)$ based on the direction dependent tunneling distance $\lambda/\cos(\theta)$ and effective mass $m^*(\theta)$, and integrate over the full range of transport directions to obtain the total BTBT current I_{ON}. Considering the effective masses anisotropy in BP, the tunneling direction dependent effective mass $m^*(\theta)$ is estimated by assuming an elliptical iso-energy surface in k-space. Figure S6(b) shows the results of the model. The dependence of ON-current on the orientation of the BP device shows a strong non-linear behavior. However, while the possible range of I_{max}/I between transport in the armchair and in the zigzag direction can be as much as ~10^3, the ON-current differs only by less than 50% when the transport direction is within 30° of the armchair direction.

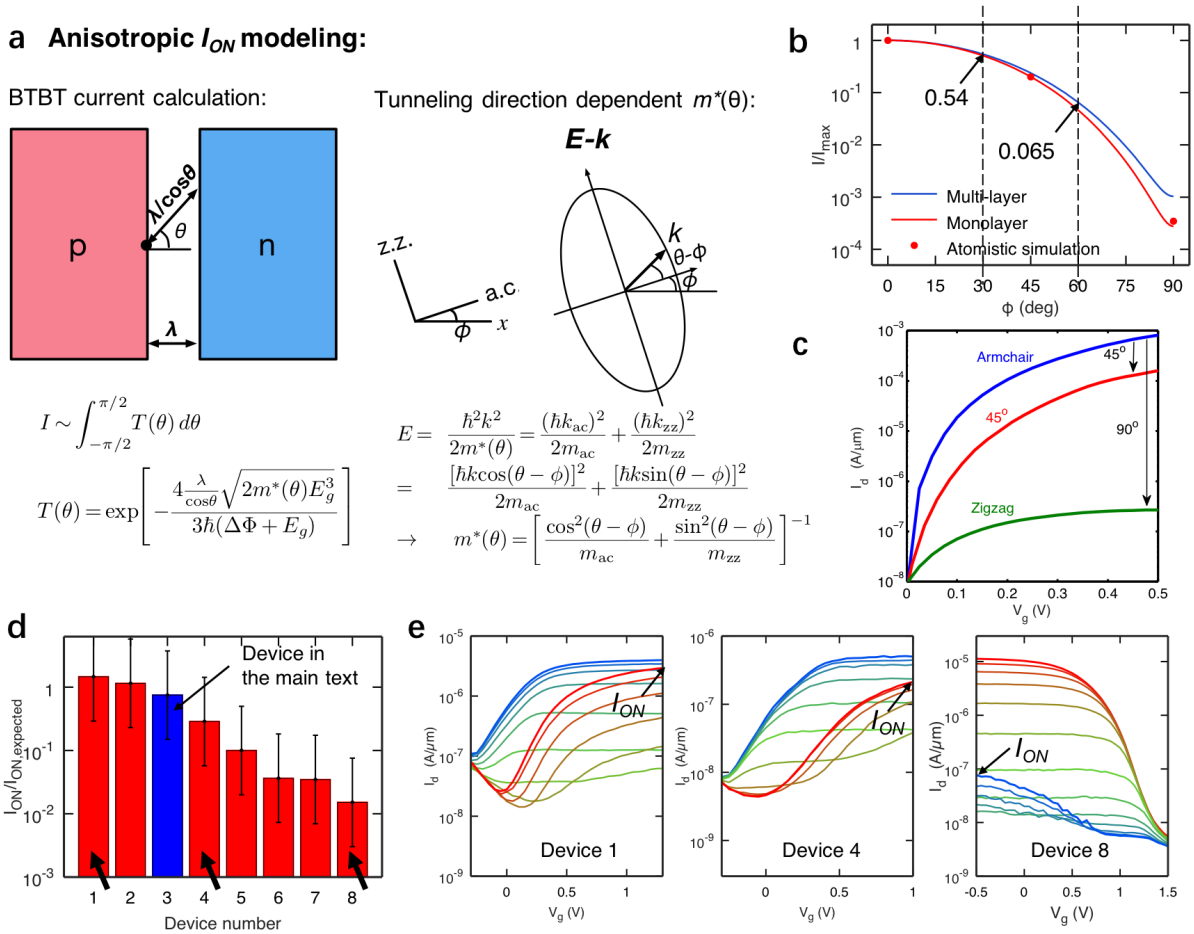

Figure S6. Effects of BP orientation and transport direction on BTBT. (a) Brief description of modeling approach of orientation-dependent BTBT current in BP TFETs. (b). Orientation-dependent I_{ON} of multi-layer and mono-layer BP TFETs from the model. The results match with atomistic simulation. (c) Atomistic simulation of effects of BP orientation on BTBT in a mono-layer TFET with EOT=0.5nm. (d) Statistics of I_{ON} of experimental devices, normalized by expected I_{ON}. (e) Exemplary device characteristics from the statistics in (d).

Figure S6(c) shows atomistic simulations of I_d-V_g curves for a BP TFET along different transport directions. The thickness of BP in the simulation is assumed to be that of a single mono-layer and the gate oxide is HfO_2 with an EOT = 0.5 nm with the spacer between separate gates etched away. This simulation has not been performed for the larger flake thicknesses since a reduced symmetry in the structure along the transverse direction significantly increases the computational cost, which makes it unfeasible to perform simulations with thicker cross-sections. This point can however be addressed by the analytic modeling approach shown in Figure S6(a). The atomistic simulation results match well with the analytical model, as shown by the red dots and line in Figure S6(b).

We have further investigated the effects of orientation on the ON-currents in BP TFET through a statistical study of our experimental data. In the experiments, the orientation of BP is not controlled deliberately; therefore, one can assume the orientation of BP to be randomly distributed between 0° to 90°. Figure S6(d) shows the statistical distribution of ON-currents of experimental BP TFETs, normalized by the "expected" ON-current values. The "expected" ON-current values are estimated from the body thickness of the BP flake, assuming that transport is

along the armchair direction. Note that since these devices share the same triple-gate structure, the main factors affecting ON-currents are the bandgap and the screening length λ, which can be deduced from the body thickness of the individual devices. In Figure S6(d) we assign an error bar of 5X to the expected ON-current, considering the uncertainty in body thickness estimation. One can see that the distribution matches approximately with the orientation-dependent trend from our analytic model shown in Figure S6(b). The device investigated in the main text, indicated by the blue bar, falls into the category of less than 50% deviation from the armchair direction, *i.e.*, the transport direction is expected to be within 30° of the armchair direction. However, the eight devices explored by us cover indeed the expected range of ON-currents for differently oriented BP TFETs. In order to control the orientation of BP more precisely, one could envision determining the orientation of BP using angle-dependent Raman spectroscopy prior to device fabrication and alignment of the channel in the armchair direction.[9]

Figure S6(e) shows exemplary device characteristics of the devices indicated by the black arrows from the statistical study shown in Figure S6(d). It is worth mentioning that in Device 8, the BTBT branch is already barely observable, since the thermal current cut-off limit at room-temperature is only less than one order of magnitude lower. This implies that a device with $I_{ON}/I_{ON,expected}$ below 10^{-2} may yield a BTBT branch that is not observable at all, which is likely the reason why lower currents as predicted by Figure S6(b) were not observed in Figure S6(d).

7. Scaling of vertical and lateral TFETs

Figure S7 shows a qualitative comparison of the scaling properties of a vertical TFET and a lateral TFET. One can easily see that since the tunneling area in a vertical TFET is proportional to the channel length L, the normalized ON-current will decrease proportionally when scaling down the channel length, as shown in Figure S7(a). Moreover, the accessible steep slope regime will also decrease after scaling. By contrast, the ON-current of a lateral device will not be affected by channel length scaling, as shown in Figure S7(b). Therefore, lateral TFETs have better scaling potential than vertical TFETs.

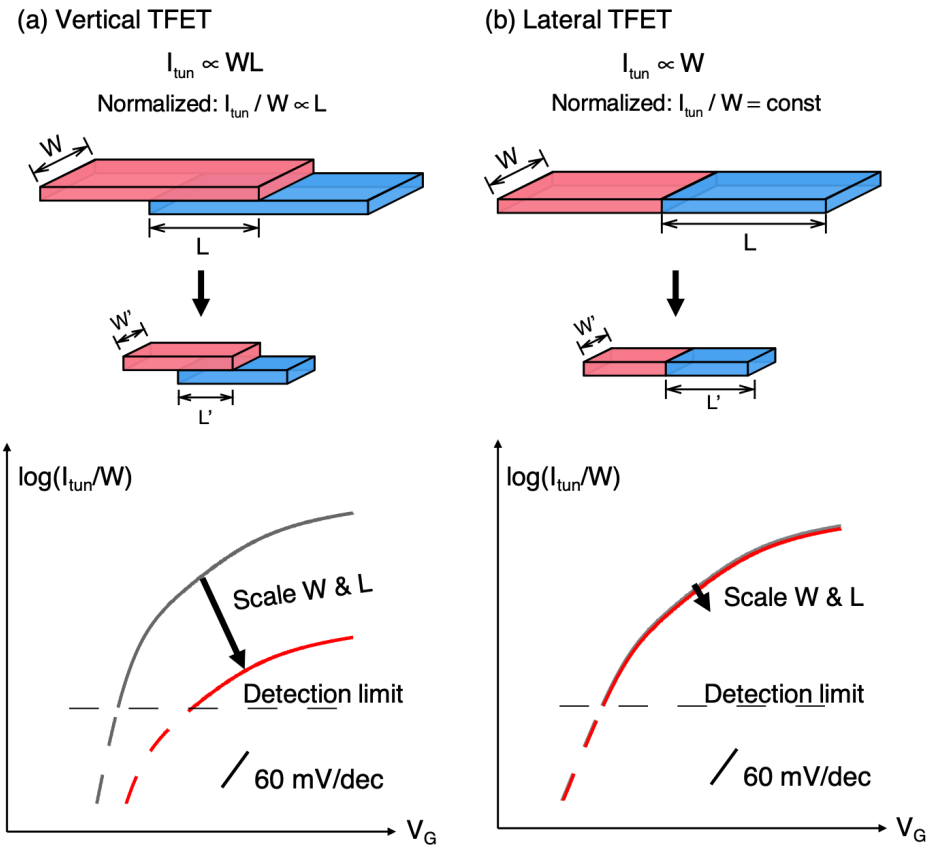

Figure S7. Comparison of scaling for (a) a vertical TFET and (b) a lateral TFET

8. Device structure and characteristics of an earlier prototype device

Figure S8 shows the device structure and characteristics of an earlier prototype device (denoted as "Exp. 2" in Figure 5a in main text). Figure S8(a) shows the schematic and SEM image of the device. The device structure is similar to the BP RED-TFET in the main text, except that the dielectric is composed of a 1.2 nm SiO_2/5 nm Al_2O_3 stack, instead of the HfO_2/Al_2O_3 stack in the main text. Figure S8(b) shows an AFM image and a line scan of the BP flake used for the device, showing an apparent thickness of t_{body}=12.8 nm. According to the analysis in the Supplementary Section 1, the PO_x formation means that this device has a real body and oxide thickness of t'_{body}=7 nm and t'_{ox}=8.1 nm, numbers that were used in the simulation shown in Figure 5a. Figure S8(c, d) show the transfer characteristics of the device in n-type and p-type configurations, respectively. By tuning the source or drain doping conditions, transitions from the MOSFET modes to the TFET modes are observed. Figure S8(e, f) shows the band diagrams of the device in the n-type and p-type configurations, showing the transitions from the MOSFET modes to the TFET modes.

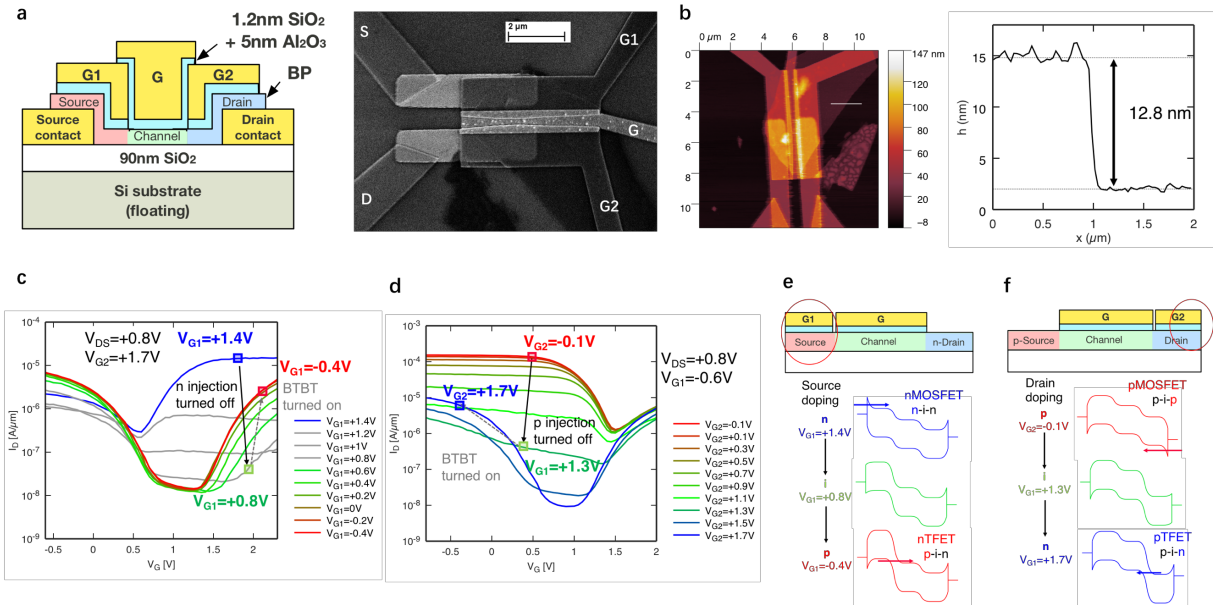

Figure S8. (a) Schematic and SEM image of an earlier prototype device (Exp. 2 in Figure 5). (b) AFM image and line scan of the BP flake, showing an apparent BP thickness of 12.8 nm. (c, d) Transfer characteristics of the device in (c) n-type and (d) p-type configurations under different (c) source (d) drain doping conditions, showing the transition from the MOSFET mode to the TFET mode. (e, f) Band diagrams of the device in (c) n-type and (d) p-type configurations corresponding to different source or drain doping conditions.

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