Transfer characteristics and low-frequency noise in single- and multi-layer MoS_2 field-effect transistors

Deepak Sharma,[1,2,3] Abhishek Motayed,[1,4] Pankaj B. Shah,[5] Matin Amani,[5] Mariela Georgieva,[5] A. Glen Birdwell,[5] Madan Dubey,[5] Qiliang Li,[3] and Albert V. Davydov[1]
[1]*Material Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA*
[2]*Theiss Research, Inc., La Jolla, California 92037, USA*
[3]*Department of Electrical and Computer Engineering, George Mason University, Fairfax, Virginia 22030, USA*
[4]*IREAP, University of Maryland, College Park, Maryland 20742, USA*
[5]*Sensors and Electron Devices Directorate, Army Research Laboratory, Adelphi, Maryland 20783, USA*

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Leveraging nanoscale field-effect transistors (FETs) in integrated circuits depends heavily on its transfer characteristics and low-frequency noise (LFN) properties. Here, we report the transfer characteristics and LFN in FETs fabricated with molybdenum disulfide (MoS_2) with different layer (L) counts. 4L to 6L devices showed highest I_{ON}-I_{OFF} ratio ($\approx 10^8$) whereas LFN was maximum for 1L device with normalized power spectral density (PSD) $\approx 1.5 \times 10^{-5}\,Hz^{-1}$. For devices with $L \approx 6$, PSD was minimum ($\approx 2 \times 10^{-8}\,Hz^{-1}$). Further, LFN for single and few layer devices satisfied carrier number fluctuation (CNF) model in both weak and strong accumulation regimes while thicker devices followed Hooge's mobility fluctuation model in the weak accumulation regime and CNF model in strong accumulation regime, respectively. Transfer-characteristics and LFN experimental data are explained with the help of model incorporating Thomas-Fermi charge screening and inter-layer resistance coupling. © *2015 AIP Publishing LLC*.
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Two-dimension (2D) materials are gaining considerable attention due to their usefulness in several fields such as chemical sensing, optoelectronic, digital electronics, and valley polarization.[1–6] These single- and few-atom thick layered materials have significant advantages provided that the key challenges related to their growth and device fabrication processes can be solved. For several electronic applications, field-effect transistors (FETs) fabricated from MoS_2 and related transition metal dichalcogenide (TMDC) layers are considered good candidates. MoS_2 has a direct, 1.8 eV, and indirect, 1.2 eV, band gap for single- and multi-layer films, respectively, and large, 200–500 $cm^2\,V^{-1}\,s^{-1}$, carrier mobility values. These properties combined with high current on-off ratio ($>10^8$) and sub-threshold swing close to 60 mV/decade for MoS_2 FETs are encouraging from circuit design aspect.[1,5,7,8] One of the requirements for efficient FETs is the low magnitude of low-frequency noise (LFN). Flicker (*1/f*) noise is a major contributor to the LFN, and it increases as the reciprocal of the device area and becomes a major concern for deeply scaled devices.[9] Moreover, excessive LFN adversely impacts the performance of analog and digital circuits. The *1/f* noise also imposes limitation on RF circuit design as it gives rise to phase noise in oscillators and multiplexers.[10,11] Lately, few groups have studied LFN in MoS_2 FETs.[12–19] In single- to few-layer FETs, it has been explained by Hooge's mobility fluctuation (HMF) model,[12] or, alternatively, by carrier number fluctuation (CNF) model,[13–17] or by a unified model, incorporating CNF and correlated surface mobility fluctuation mechanisms.[18] In thicker layer FETs, LFN has been associated with CNF,[16,19] or with a combination of CNF and HMF.[13] While these results are insightful, it is essential to correlate the measured LFN data with the FET operation regimes to gain most accurate understanding of the origin of low-frequency noise in 2D transistors. To provide an insight and to help guiding device design and optimization, this paper analyses how the FET operating regimes relate to the LFN mechanisms depending on the number of MoS_2 device layers.

In this study, we examine the transport and LFN properties in back-gated FETs fabricated from mechanically exfoliated MoS_2 with systematically varied layer counts, ranging from single- (~0.7 nm) to multi- (~20 nm) layer (see the supplementary material for the fabrication steps).[20] Our electrical and LFN experimental findings clearly suggested that devices with thickness around 4L to 6L give the best FET performance. Study on the origin of LFN with the help of CNF and HMF models further revealed contrasting mechanisms in few-layer vs. multi-layer FETs. These behaviors are representative of at least three sets of FETs for each layer thickness studied here. We further linked the transfer characteristics and LFN results together to explain the transport mechanism with the help of a model incorporating Thomas-Fermi charge screening and inter-layer resistance coupling.

Figs. 1(a), 1(b), and 1(c) show the top-view schematic, scanning electron microscope (SEM) plan-view image, and cross-sectional schematic of the device, respectively. Fig. 1(d) shows the resistor network model (explained later in the paper) of the fabricated devices. For ease of discussion, we will refer to MoS_2 FETs with $L < 9$ as "few-layer" devices, and $L \geq 9$ as "thick" devices. In addition, for any quantity represented here the subscript n denotes the value for the n_{th} layer, with $n = 1$ being the layer closest to the gate oxide.

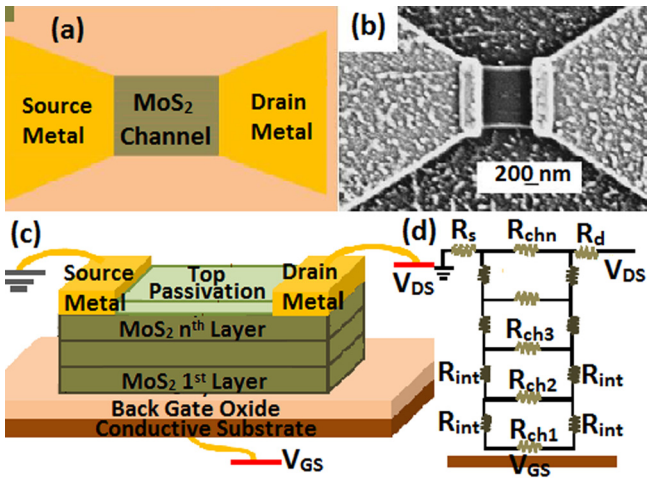

FIG. 1. Few-layer MoS_2 FETs: (a) Top view schematics, (b) SEM plan-view image, (c) cross-sectional schematics, and (d) equivalent resistor model network.

Details about the experimental setup and methods can be found in our previous paper.[18]

(a) Electrical transport: Fig. 2(a) shows the normalized I_{DS} vs. V_{DS} characteristics at $V_{GS} = 30$ V for four different devices at 300 K. As expected, devices with more layers had greater channel currents, although I_{DS} eventually decreases for thicker devices. This thickness dependent behavior of device conductance (G) is interesting since intuitively G should increase with increasing channel thickness. It is worth pointing out that multi-layer MoS_2 should have a large current density due to its lower band-gap and three times higher density of states at the conduction band minima as compared to 1L MoS_2.[21,22] Two-terminal resistance (R) measurements (at $V_{GS} = 30$ V) for different devices as a function of MoS_2 layer count show (Fig. 2(b)) the unusual trend of variation of G ($G = 1/R$) with channel thickness.

We calculated the field-effect mobility values of 14.7, 16.7, and 15.3 $cm^2/V{\cdot}s$ for 1L, 2L, and thick devices, respectively, via four-point probe measurements. It is worth mentioning that estimation of mobility from measurement of MoS_2 FETs is prone to errors due to the factors such as contribution of high contact resistances (which is eliminated in case of four-point probe measurements) and error in the estimation of gate capacitance. The transfer characteristic plot for different devices is shown in Fig. 3(a). It is evident that all the devices show depletion mode n-channel behavior. We refer to I_{DS} as I_{OFF} in the region where G is low ($V_{GS} < V_{TH}$) and as I_{ON} in the region where G is high ($V_{GS} \gg V_{TH}$), where V_{TH} represents the threshold voltage of the FETs. As expected, our measurements show that I_{OFF} increases gradually with increasing channel thickness. On the other hand, I_{ON} initially increases with channel thickness but then decreases for thicker devices. Interestingly, in case of Graphene FETs, I_{ON}-I_{OFF} ratio vs channel thickness shows 1/thickness dependence.[23]

(b) Low-frequency noise: To gain more insight into the nature of conduction, we performed LFN measurements on these FETs. The normalized drain current power spectral density (PSD) ($=S_{ID}/I_{DS}^2$) at $V_{DS} = 0.5$ V and $V_{GS} = 60$ V for different layer thicknesses is shown in Fig. 4(a). Fig. 4(b) shows the normalized PSD value at 10 Hz vs the channel thickness. From Fig. 4(b), it is evident that maximum LFN

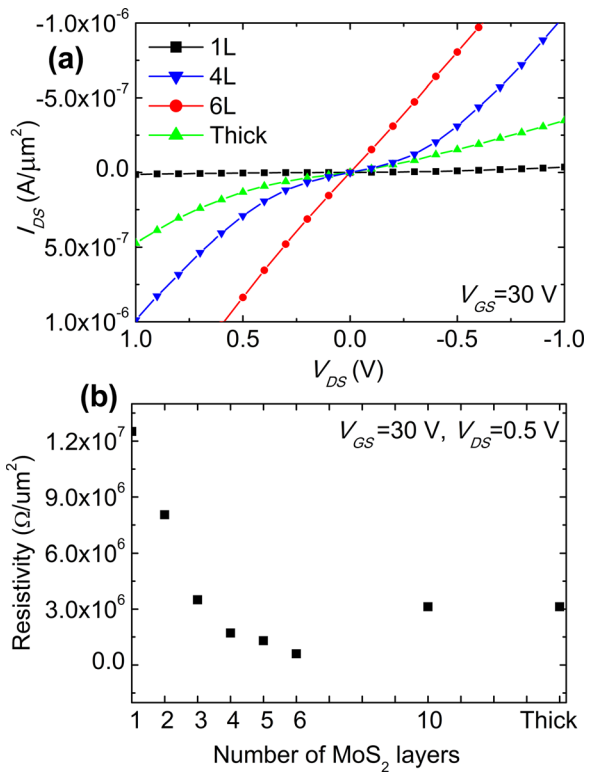

FIG. 2. (a) I_{DS}-V_{DS} plot for the FETs with different number of MoS_2 layers, (b) two-terminal resistivity plot for the FETs with different number of layers. All the I-V curves were taken at constant gate-source voltage ($V_{GS} = 30$ V).

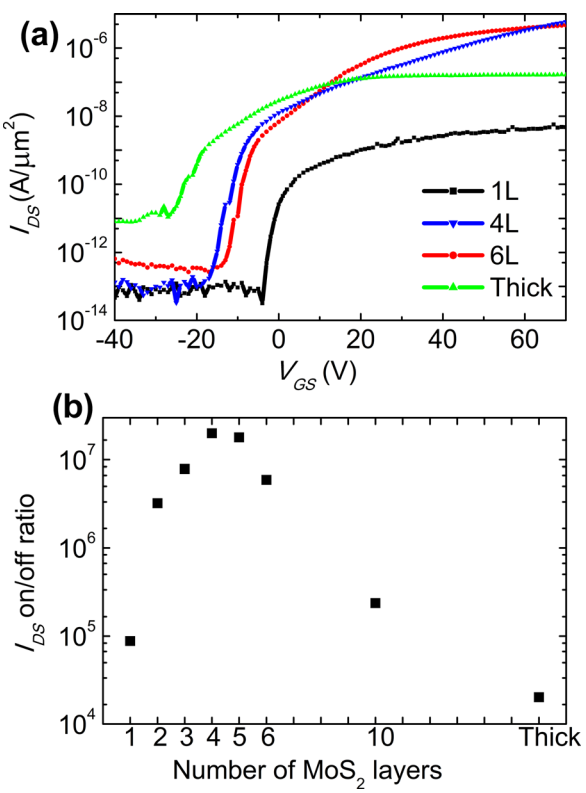

FIG. 3. (a) Transfer characteristics and (b) I_{ON}-I_{OFF} ratio for the FETs with different number of MoS_2 layers. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

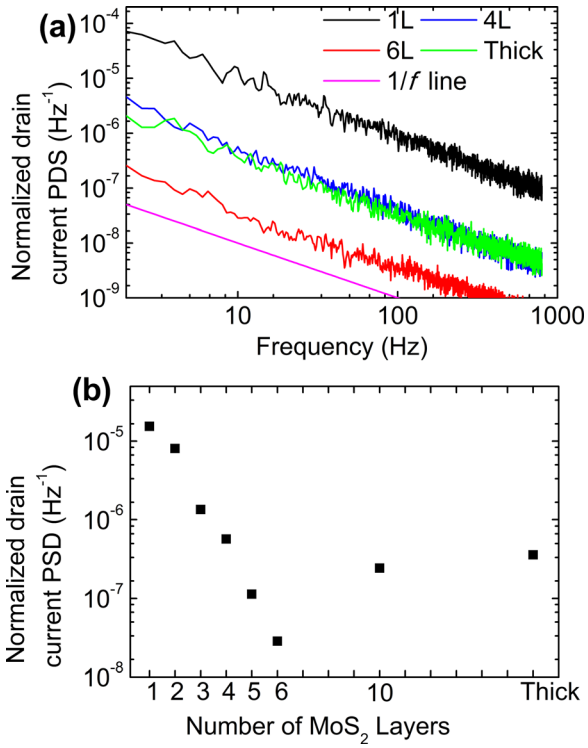

FIG. 4. (a) Normalized PSD of the drain current and (b) magnitude of normalized PSD of the drain current at 10 Hz, for FETs with different number of MoS_2 layers. All the readings were taken at a constant drain-source voltage ($V_{DS}=0.5$ V) and gate-source voltage ($V_{GS}=60$ V). A $1/f$ straight line in (a) is shown for comparison.

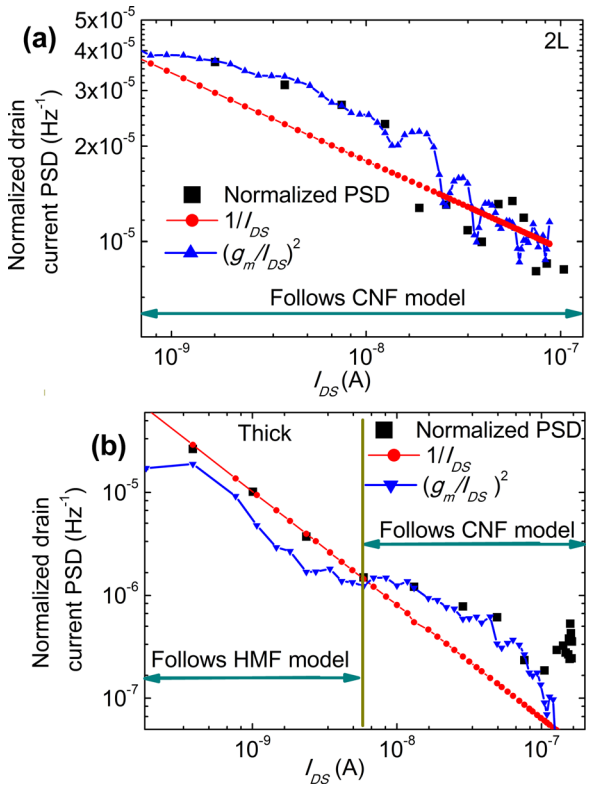

FIG. 5. Plot of three different parameters: normalized PSD of the drain current at $f=10$ Hz, $(g_m/I_{DS})^2$, and $1/I_{DS}$, as a function of I_{DS}. (a) for a 2L FET and (b) for a thick device. All the readings were taken at a constant drain-source voltage ($V_{DS}=0.5$ V). Note: absolute values of $(g_m/I_{DS})^2$ and $1/I_{DS}$ are not shown in the plots.

occurs in the 1L device and decreases significantly with the increase in channel thickness, and eventually shows a slight increase for thicker devices. All the experimental LFN data closely followed the $1/f$ trend.

To reveal the origins of LFN fluctuations, we plotted S_{ID}/I_{DS}^2 vs I_{DS} in a log-log scale. If S_{ID}/I_{DS}^2 varies with I_{DS} as $(g_m/I_{DS})^2$, where g_m is the transconductance, the CNF model is better suited to explain the dominant source of the $1/f$ noise. Note that in our previous paper, we explained LFN in a single-layer MoS_2 FET using the unified model.[18] Since the unified model is essentially the CNF model incorporating correlated surface mobility fluctuation effects, here we use the CNF model for simplicity. On the other hand, if S_{ID}/I_{DS}^2 is proportional to $1/I_{DS}$ then HMF model explains LFN more accurately.[24–26] The CNF model is based on surface effects, i.e., LFN is dominated by trapping and de-trapping of free carriers by the oxide-semiconductor interface traps;[25–27] whereas HMF model suggests that LFN is a bulk phenomenon, i.e., LFN is caused by fluctuation of bulk mobility induced by fluctuations in phonon population.[9,24,25] Figs. 5(a) and 5(b) show S_{ID}/I_{DS}^2 vs I_{DS} plot in log-log scale. For easy analysis, $(g_m/I_{DS})^2$ vs I_{DS} and $1/I_{DS}$ vs I_{DS} are also plotted in the same figure, with $(g_m/I_{DS})^2$ and $1/I_{DS}$ values scaled accordingly to fit with S_{ID}/I_{DS}^2 data points with common x-axis as I_{DS}. The absolute values of $(g_m/I_{DS})^2$ and $1/I_{DS}$ are not shown in Figs. 5(a) and 5(b) as they are not important for our discussion. From Fig. 5(a), it is evident that LFN in 2L FET follows CNF model closely implying dominant LFN due to surface conduction. A similar trend was seen in all the few-layer devices. However, Fig. 5(b) suggests that LFN in thicker devices follows CNF model closely at high V_{GS} (strong accumulation regime where I_{DS} is high) implying LFN dominated by surface conduction, but tends to follow HMF model at low V_{GS} (weak accumulation regime where I_{DS} is low) implying LFN dominated by bulk conduction. The contrast in the measured LFN results for fewer-layer vs. thicker devices is interesting. Na *et al.* in their paper had shown that LFN in thick (~11.3 nm) MoS_2 devices is a result of a combination of both HMF and CNF models, while in bulk (~40 nm) MoS_2 devices LFN closely followed the HMF model.[13] Based on this paper findings, Table I summarizes the model describing the LFN in MoS_2 FETs with different channel thicknesses.

Previously, conduction in Graphene FETs had been explained using a model (here, we call it model B) incorporating Thomas-Fermi (T-F) charge screening and inter-layer resistance coupling.[23] Das and Appenzeller also explained the conduction mechanism in multi-layer MoS_2 FETs with the help of model B.[28,29] In our work, we relate the experimental findings of transfer-characteristics and LFN together

TABLE I. Different models describing LFN dominant mechanisms in different regions of MoS_2 FETs as a function of channel layer thickness.

MoS_2 FETs	Weak-accumulation/ subthreshold regime	Strong-accumulation regime
Single and few-layer	CNF	CNF
Thick	HMF	CNF
Bulk[13]	HMF	HMF

to explain the conduction mechanism in FETs for varying channel thickness. Fig. 1(d) shows the resistor network model of a multi-layer MoS_2 FET system. Any two adjacent layers of MoS_2 are coupled by weak van der Waals forces and possess a finite inter-layer resistance (R_{int}). R_{chn}, R_s, and R_d represent the channel, source, and drain contact resistances, respectively. It is assumed that the source and drain contacts inject charge carriers from the top MoS_2 layer only since (a) top surface MoS_2-metal contact area is significantly higher than contacts with the edges of the MoS_2 layers, and (b) source and drain contacts were deposited at room temperature and FETs were not annealed preventing any diffusion of metals into MoS_2. Apart from utilizing resistor model network, model B takes T-F charge screening effect into account according to which distribution of the charge among various channel layers can be estimated by

$$\frac{Q_n}{Q_{n-1}} \approx \exp\left(-\frac{\Delta x}{\lambda}\right) \quad \text{and} \quad \sum_{n=1}^{N} Q_n = Q_{gate}, \tag{1}$$

where Δx is the distance between two consecutive layers, λ is the charge screening length, Q is the total charge under screening, and Q_{gate} is the total charge on the gate [$Q_{gate} = C_{OX}(V_{GS} - V_{TH})$].[23,28,29] It is evident from Eq. (1) that the smaller the value of λ compared to Δx, the lower the charge concentration will be in the layer closest to the gate oxide. In case of MoS_2 FETs several values of λ have been used ranging from 3 nm to 8 nm.[8,28,30] These values of λ were estimated for FETs without top surface passivation. Since in our devices top surface is passivated with Al_2O_3, there may be an additional field pushing the charge carriers to MoS_2 layers closer to the gate oxide, resulting in effective lower value of λ. For Graphene FETs, λ is quite small ($\approx$0.7 nm).[23,31] Now, in our case I_{ON} and I_{OFF} both increased with increasing L for few-layer devices. The increase in both I_{ON} and I_{OFF} is simply a result of additional parallel conduction paths. LFN follows the CNF model suggesting that dominant fluctuation in conduction is in the layer closer to back gate oxide (expected for few layer devices and shown in Fig. 5(a)). Model B predicts the similar results assuming large λ ($\gg$1L thickness) and some constant R_{int}. LFN is significantly higher and mobility is expected to be lower due to charge scattering at the gate oxide interfaces. For thicker devices, I_{ON} decreases with thickness while I_{OFF} tends to show a steady increase. Consequently, I_{ON}-I_{OFF} ratio goes down with the increase in the thickness. Both R_{int} and λ are the limiting factors for thicker devices. R_{int} prevents the current to penetrate below few layers from the top of the MoS_2 stack. This results in both I_{ON} and I_{OFF} increasing very slowly with thickness and eventually becoming constant for very thick, i.e., bulk-like, devices. Furthermore, when FET is in on state charge screening effect tends to decrease the conductance (lower number of charge carriers) in the first few layers from the top of the thick MoS_2 stack. This effectively results in the overall decrease in I_{ON} with thickness (Figs. 2 and 3). In strong-accumulation regime, LFN followed CNF model suggesting that LFN is dominated by the carrier fluctuations at the gate oxide interface. Although, in weak accumulation regime, LFN tends to follow HMF model closely, suggesting bulk mobility fluctuation as the dominant source of LFN (Fig. 5(b)). Since at low gate bias ($V_{GS} \approx 0$), the charge carriers are not concentrated near the gate oxide and large number of layers (now with much higher R_{chn}) contribute to I_{DS}, it is not surprising to see LFN following HMF model. For very thick devices, we can expect HMF to be dominant in all regions of operation since there will be less contribution of the MoS_2 layers, which are closer to back gate oxide to the overall conductance (Table I) as shown by Na *et al.*[13] Most of the recent literature agrees with our finding that CNF model is the dominant source of noise in thin and thick MoS_2 FETs, especially at high V_{GS} values.[13–19] At low V_{GS} values, LFN levels go much higher for both thin and thick layer devices (Fig. 5) to become comparable to each other.[16] In this paper, we reveal how the LFN mechanism changes as a function of the device layer thickness in different regions of FET operation.

In conclusion, we presented our experimental results of transfer characteristics and LFN measurements of MoS_2 FETs with different channel thickness. Transfer characteristics show that I_{OFF} increased with channel thickness; I_{ON} on the other hand showed an initial increase and then eventually started to decrease for thicker devices. LFN was found to be maximum for devices with $L < 4$. Few-layer devices followed CNF model in all regimes suggesting that LFN is mainly due to carrier number fluctuations at gate oxide interface. LFN was significantly reduced for $L > 3$ devices. LFN in thicker devices followed CNF model in strong accumulation regime and HMF model in weak accumulation regime suggesting bulk mobility fluctuation as a dominant source of noise. We explained electrical transport in these devices by incorporating Thomas-Fermi (T-F) charge screening and inter-layer resistance coupling in the model. MoS_2 FETs with 4L to 6L gave best performance in terms of both transfer characteristics and LFN. Thick devices suffered from comparatively low I_{ON}-I_{OFF} ratio, weak dependence of channel current on V_{GS}, and slight increase in LFN, while conduction in 1L-3L FETs suffer from low mobility and high LFN likely due to presence of surface states at the oxide-semiconductor interface.

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[1]H. Wang, L. L. Yu, Y. H. Lee, Y. M. Shi, A. Hsu, M. L. Chin, L. J. Li, M. Dubey, J. Kong, and T. Palacios, Nano Lett. **12**, 4674 (2012).
[2]Z. P. Sun, T. Hasan, F. Torrisi, D. Popa, G. Privitera, F. Q. Wang, F. Bonaccorso, D. M. Basko, and A. C. Ferrari, ACS Nano **4**, 803 (2010).
[3]F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[4]B. Radisavljevic, M. B. Whitwick, and A. Kis, ACS Nano **5**, 9934 (2011).
[5]N. Ivanovic, I. Radisavljevic, N. Novakovic, M. Manasijevic, and D. Colognesi, Acta Phys. Pol. A **120**, 242 (2011).

[6]K. F. Mak, K. L. He, J. Shan, and T. F. Heinz, Nat. Nanotechnol. **7**, 494 (2012).
[7]K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, Phys. Rev. Lett. **105**, 136805 (2010).
[8]S. Das, H. Y. Chen, A. V. Penumatcha, and J. Appenzeller, Nano Lett. **13**, 100 (2013).
[9]F. N. Hooge, Physica B & C **83**, 14 (1976).
[10]S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. A. J. M. van Tuijl, and B. Nauta, IEEE J. Solid-State Circuits **34**, 1022 (1999).
[11]Y. Nemirovsky, I. Brouk, and C. G. Jakobson, IEEE Trans. Electron Devices **48**, 921 (2001).
[12]V. K. Sangwan, H. N. Arnold, D. Jariwala, T. J. Marks, L. J. Lauhon, and M. C. Hersam, Nano Lett. **13**, 4351 (2013).
[13]J. Na, M. K. Joo, M. Shin, J. Huh, J. S. Kim, M. Piao, J. E. Jin, H. K. Jang, H. J. Choi, J. H. Shim, and G. T. Kim, Nanoscale **6**, 433 (2014).
[14]J. Renteria, R. Samnakay, S. L. Rumyantsev, P. Goli, M. S. Shur, and A. A. Balandin, Appl. Phys. Lett. **104**, 153104 (2014).
[15]X. J. Xie, D. Sarkar, W. Liu, J. H. Kang, O. Marinov, M. J. Deen, and K. Banerjee, ACS Nano **8**, 5633 (2014).
[16]S. L. Rumyantsev, C. Jiang, R. Samnakay, M. S. Shur, and A. A. Balandin, IEEE Electron Device Lett. **36**, 517 (2015).
[17]S. Ghatak, S. Mukherjee, M. Jain, D. D. Sarma, and A. Ghosh, APL Mater. **2**, 092515 (2014).
[18]D. Sharma, M. Amani, A. Motayed, P. B. Shah, A. G. Birdwell, S. Najmaei, P. M. Ajayan, J. Lou, M. Dubey, Q. Li, and A. V. Davydov, Nanotechnology **25**, 155702 (2014).
[19]H.-J. Kwon, H. Kang, J. Jang, S. Kim, and C. P. Grigoropoulos, Appl. Phys. Lett. **104**, 083110 (2014).
[20]See supplementary material at http://dx.doi.org/10.1063/1.4932945 for the device fabrication steps.
[21]S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J. B. Yoo, J. Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, Nat. Commun. **3**, 1011 (2012).
[22]J. T. Ye, Y. J. Zhang, Y. Matsuhashi, and Y. Iwasa, Nano Lett. **12**, 1136 (2012).
[23]Y. Sui and J. Appenzeller, Nano Lett. **9**, 2973 (2009).
[24]G. Ghibaudo, Proc. SPIE **5113**, 16 (2003).
[25]K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, IEEE Trans. Electron Devices **37**, 654 (1990).
[26]G. Ghibaudo, O. Roux, C. Nguyenduc, F. Balestra, and J. Brini, Phys. Status Solidi A **124**, 571 (1991).
[27]A. L. McWhorter, Ph.D. Thesis, Massachusetts Institute of Technology, 1955, available at http://hdl.handle.net/1721.1/12061.
[28]S. Das and J. Appenzeller, Phys. Status Solidi RRL **7**, 268 (2013).
[29]S. Das and J. Appenzeller, Nano Lett. **13**, 3396 (2013).
[30]Y. Li, C. Y. Xu, and L. Zhen, Appl. Phys. Lett. **102**, 143110 (2013).
[31]F. Guinea, Phys. Rev. B **75**, 235433 (2007).

Supplemental Information

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Deepak Sharma [1-3], Abhishek Motayed [1,4], Pankaj B Shah [5], Matin Amani [5], Mariela Georgieva [5], A Glen Birdwell [5], Madan Dubey [5], Qiliang Li,[3] and Albert V Davydov [1]

[1]National Institute of Standards and Technology, Material Measurement Laboratory, Gaithersburg, MD 20899, USA

[2]Theiss Research, Inc., La Jolla, CA 92037, USA

[3]Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030, USA

[4]IREAP, University of Maryland, College Park, MD 20742, USA

[5]Sensors and Electron Devices Directorate, Army Research Laboratory, Adelphi, MD 20783, USA

MoS_2 films of various thicknesses were obtained by micromechanical exfoliation on a heavily doped Si substrate with a 300 nm SiO_2. Layers with various thicknesses were located by optical microscopy and the L count was estimated by Raman and PL spectroscopy. Back-gated transistors were then fabricated on various MoS_2 flakes using electron-beam lithography (EBL). Devices were patterned using a low power reactive ion etch in a CH_4/O_2 plasma and Ti/Au (15/85 nm) contacts were subsequently deposited using electron beam evaporation. A 20 nm thick Al_2O_3 dielectric was deposited over the samples using atomic layer deposition (ALD). Both channel length and width of all the FETs were 1μm.