GaN-nanowire/amorphous-Si core-shell heterojunction diodes

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We report the electrical characterization of gallium-nitride/amorphous-silicon (*n*-type nanowire/*p*-type shell) diodes fabricated by postgrowth silicon shell formation technique. The *n*-type (unintentionally doped) gallium-nitride (GaN) nanowires were aligned on prepatterned sapphire substrates using dielectrophoresis. The amorphous silicon (*a*-Si) shell was deposited using plasma enhanced chemical vapor deposition technique and doped using spin-on boron dopant. Using photolithography, plasma etching, and metal deposition, complete *p-n* (*p*-type *a*-Si shell on *n*-type GaN nanowire) heterojunction diodes were developed. These diodes had reliable electrical characteristics with 1 V forward turn-on voltage. These nanowire core-shell heterojunction diodes exhibited negative differential resistance, which can be explained by phonon-assisted interband tunneling mechanism. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3021390]

Semiconducting nanowire based devices have already shown their merits in terms of performance and functionality.[1] Apart from superior device characteristics, nanowire based electronic and photonic devices also provide the way for "heterointegration"—assembling devices realized from different materials with specific functionalities on a single substrate for complex system-on-a-chip solutions. In order to develop such systems we need nanowire based subcomponents such as diodes, transistors, light emitters, and detectors. The group III-nitride (Al/Ga/In–N) material system with its unique properties[2] (i.e., direct bandgap spanning the entire solar spectrum, existence of ternary and quaternary alloys, high-temperature/power/frequency operation) offers an opportunity for developing the next generation of nanowire based electronic and optical components. The realization of nanowire based *p-n* junctions is specifically important as these junctions form the basis for devices including light-emitting diodes, bipolar transistors, lasers, detectors, and sensors. The most efficient design of a nanowire based *p-n* junction is a core-shell structure, where the injection occurs uniformly over the entire cross section of the nanowire.[3] Unfortunately it is often difficult to control the growth and dopant concentration in such a structure. A simpler alternative is to place a nanowire of a specific conductivity type (*n* or *p*-type) in contact with a substrate of different conductivity type, thus forming a mechanical *p-n* junction.[4,5] This method offers a simple and flexible solution but lacks the efficiency of an epitaxially formed junction. Such structures are often plagued with nonidealities arising from interfacial oxides and defects.[5]

We have realized nanowire based core-shell heterojunction diodes using *n*-type gallium-nitride (GaN) nanowires as the cores with *p*-type amorphous silicon (*a*-Si) shells surrounding them. The device is formed by dielectrophoretically aligning the nanowire on a substrate and subsequent *p*-Si shell formation. We have combined the flexibility of postgrowth fabrication together with the efficiency of silicon-compatible processing techniques to realize these nanowire core-shell diodes. Our proposed design of the GaN nanowire based *p-n* junction is a proof of concept and is applicable for other nanowire and shell systems. Reports have also shown electroluminescence from Si–GaN junctions, which is also an important motivation for the proposed study.[5,6]

GaN nanowires with diameters ranging from 50 to 300 nm and lengths up to 200 μm were grown by direct reaction of gallium vapor with flowing ammonia at 850 to 900 °C.[7] As-grown, unintentionally doped nanowires are *n*-type with carrier concentration in the range of 2×10^{18} cm^{-3}, estimated from field-effect transistor measurements.[7] The nanowires were aligned on a sapphire substrate between pairs of Ti (15 nm thick) electrodes using dielectrophoresis[7] [Fig. 1(a)]. Following the alignment, 60 nm of SiO_2 was deposited

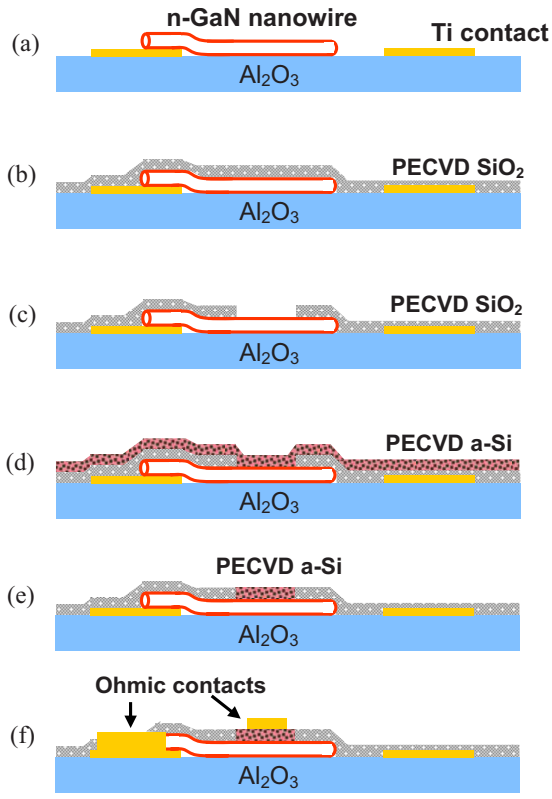

FIG. 1. (Color online) Schematic representation of the fabrication process of GaN/*a*-Si core-shell structure.

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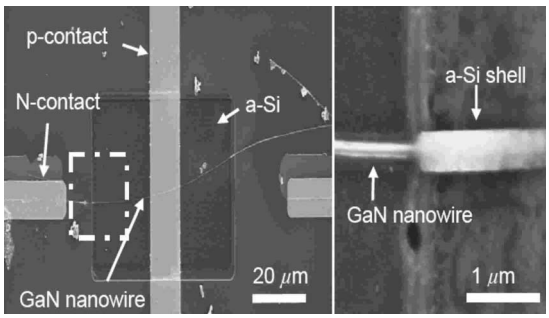

FIG. 2. (a) SEM image of a completed GaN/*a*-Si heterojunction diode. (b) High-magnification SEM image of the area highlighted in (a) by broken white square showing the core-shell nature of the completed device.

using plasma enhanced chemical vapor deposition (PECVD) on the substrate encapsulating the nanowires [Fig. 1(b)]. Using photolithography and subsequent reactive ion etching (RIE) of the SiO_2,[8] a window was opened over the nanowire [Fig. 1(c)]. This was followed by the deposition of 100 nm of *a*-Si using a PECVD process [Fig. 1(d)]. The deposition was done at 280 °C with the chamber pressure at 1 Torr, rf power of 2 W, and silane flow rate of 400 SCCM (SCCM denotes cubic centimeter per minute at STP). The deposition rate of *a*-Si was 2.5 nm/min. The as-deposited Si did not exhibit any crystalline signature in x-ray diffraction (XRD) measurement and was highly resistive. In order to introduce *p*-type dopants in the Si, Borofilm 100 from Emulsitone[9] was spin coated on the sample and then baked at 200 °C for 20 min to remove the excess solvent present in the coat. Rapid thermal annealing of the sample was carried out in nitrogen to diffuse boron into Si.[10] After completion of the diffusion process, the Si layer was patterned by photolithography and etched using RIE (Ref. 11) to define the *p*-shell around the nanowire [Fig. 1(e)]. Using photolithography, etching (to remove the SiO_2 from the nanowire), and metal deposition (Ti/Al/Ti/Au 40/100/40/40 nm), *n* and *p* contacts were formed resulting in a complete device [Fig. 1(f)].

A scanning electron microscope (SEM) image of a complete device is shown in Fig. 2, where the omega shape of the Si shell can be clearly seen. We have fabricated over 20 single nanowire devices with different ranges of doping levels of the *p*-Si shell. The current-voltage (*I-V*) characteristics of three such diodes with different *p*-shell doping levels are shown in Fig. 3. The built-in voltage (V_{bi}) of an abrupt *p-n* Si–GaN heterojunction is given by the relationship[12] $qV_{bi} = E_{gSi} - \Delta E_c - (k_BT/q)\ln(N_c/n) - (k_BT/q)\ln(N_v/p)$, where E_{gSi} is the Si bandgap, ΔE_c is the conduction band discontinuity for GaN and Si, N_c and *n* are the conduction band density of states and equilibrium electron concentration in the *n*-type GaN, respectively, N_v and *p* are the valence band density of states and equilibrium hole concentration in the *p*-type Si, respectively, *q* is the electronic charge, k_B is the Boltzmann constant, and *T* is the absolute temperature. Onset of forward conduction in these diodes started at 1.1 V, which is consistent with the built-in voltage calculation. High reverse-bias current is indicative of the nonidealities present at the heterointerface. No detectable electroluminescence was observed in these diodes even at low temperatures. Given the fact that there is a very large barrier for the holes (2.25 eV) to flow into the GaN from the Si (Fig. 3 inset), it is more

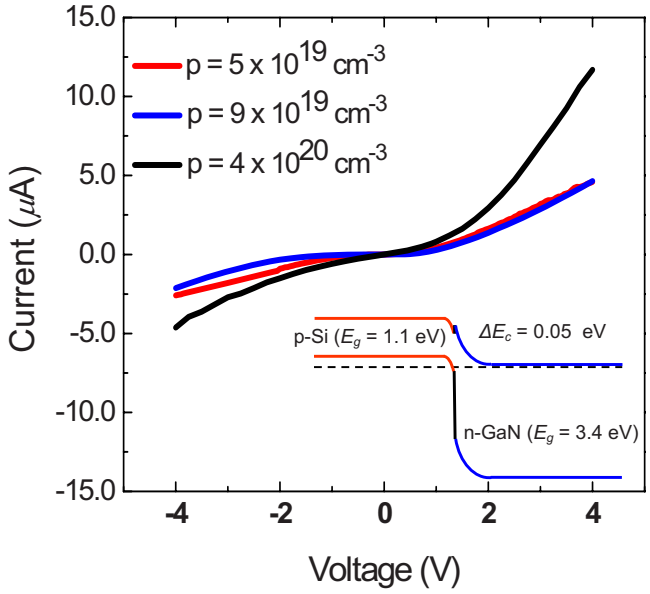

FIG. 3. (Color online) Room-temperature *I-V* characteristics of three different GaN nanowire/Si core-shell diodes with three doping levels of the *p*-Si shell. Diameters of the nanowires were in the range of 180–200 nm. (Inset) Equilibrium band alignment of *p*-Si and *n*-GaN.

favorable for the electrons to be injected from the GaN and recombine with holes in the Si. In a Si–GaN *p-n* heterojunction, the electron to hole injection current density ratio (J_n/J_p) is given by the relationship $J_n/J_p = (n\mu_n/p\mu_p) \times \exp(q\Delta E_g/k_BT)$, where μ_n and μ_p are the electron and hole mobility, respectively. For the present design J_n/J_p is about 10^{38}.

Negative differential resistance (NDR) was observed in all of the nanowire heterojunction diodes with *p*-shell doping in the range of $(8-9)\times 10^{19}$ cm^{-3}. Figure 4 is the room-temperature *I-V* characteristics of such a diode (80 nm nanowire diameter) showing NDR at both forward and reverse-bias regions. The peak to valley current ratio (I_p/I_v) is about

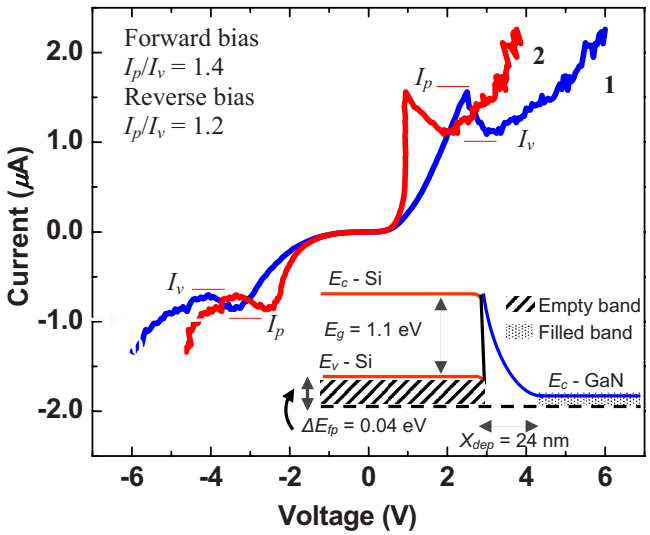

FIG. 4. (Color online) Room-temperature *I-V* characteristics of a single GaN nanowire/*a*-Si junction exhibiting NDR. The blue curve (1) is measured data and the red curve (2) is corrected for parasitic series resistance. (Inset) Equilibrium band alignment of *p*-Si and *n*-GaN showing only the alignment of Si band edges with conduction band of GaN, where ΔE_{fp} is the relative Fermi level for Si given by $(k_BT/q)\ln(N_v/p)$.

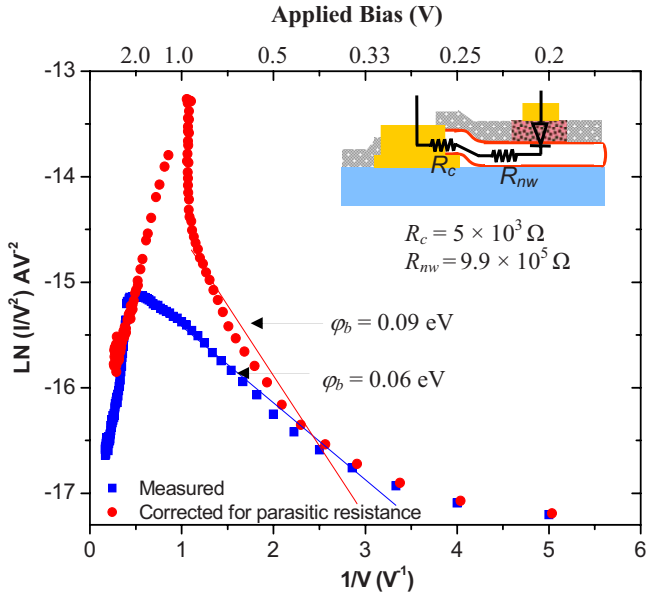

FIG. 5. (Color online) Plot of $\ln(I/V^2)$ vs $1/V$ (forward bias regime) showing the straight-line fit of the data at low voltage regime. The blue curve is for the measured data and red is for the data corrected for the parasitic series resistances. (Inset) The lumped model showing the parasitic resistances and their estimated values.

1.4 and 1.2 for forward and reverse biases, respectively. The alignment of the conduction band of GaN with respect to Si band edges as shown in the inset of Fig. 4 indicates the possibility of interband tunneling. For low forward bias ($V_f < V_{bi}$), electrons from the GaN conduction band can tunnel into the empty states in the valence band of the degenerate Si. With increased forward bias the GaN conduction band moves up and a lesser number of states are available to tunnel into, and hence the current drops, till the bias reaches the thermionic emission limit ($V_f = V_{bi}$), which results in emission over the barrier. Similarly for low reverse bias, electrons from the filled valence band of Si can tunnel into the empty states in the conduction band of GaN, whereas at higher biases the recombination and generation in the depletion region will dominate the diode current. Although the observed NDR characteristics can be qualitatively explained by the proposed mechanism, tunneling is occurring at much higher voltages than predicted by this model. One explanation could be the effect of high parasitic series resistance due to contact and nanowire resistances. A lumped model as shown in the inset of Fig. 5 with parasitic values that can be generated by measuring nanowire diameter and nanowire-contact overlap using a SEM. Contact resistance and resistivity for these nanowires have been reported earlier.[13] The *I-V* characteristic corrected for parasitic resistances is shown in Fig. 4 (curve 2), which indicates a significant change although the forward conduction voltage is still 0.5 V. Given the fact that the tunneling current starts at high bias levels, it is likely that phonon-assisted interband tunneling, which is often observed in other indirect bandgap materials, is the cause of the NDR effect in these diodes. It is possible that other mechanisms such as defect assisted tunneling or thermionic-field emission are also present. Temperature-dependent measurements are being carried out to identify the mechanism of such tunneling. From Kane's treatment,[14] the tunneling current I_T for small biases is given by the relationship

$$I_T \propto V^2 \exp\left(\frac{-\pi m^{*1/2} \varphi_b^{3/2} d}{2\sqrt{2}\hbar q V}\right), \quad (1)$$

where V is the applied bias, m^* is the effective mass of the carrier, φ_b is the barrier height, d is the width of the barrier, and $\hbar$ is the reduced Planck's constant. As evident from Eq. (1), for interband tunneling the plot of $\ln(I/V^2)$ versus $1/V$ would be a straight line with a negative slope from which the barrier height can be calculated if the barrier width is known or vice versa. In Fig. 5 $\ln(I/V^2)$ is plotted as a function of $1/V$ for the measured and parasitic resistance-corrected data for the forward bias regime. A straight line fit for both curves in the low bias regime is shown. The tunneling barrier height calculated (assuming zero-bias depletion width of 24 nm as the barrier width) from the measured data is 0.06 eV, whereas the barrier height computed from the curve corrected for parasitic resistance is about 0.09 eV. The low barrier height is not surprising considering the fact that the tunneling is occurring at high biases, where the effective tunneling barrier height is lowered.

We have demonstrated the operation of GaN nanowire/*a*-Si heterojunction diodes. These diodes were fabricated by assembling the nanowires on a substrate using dielectrophoresis and applying standard batch-fabrication techniques. The present technique can be applied to other nanowire materials and is suitable for applications requiring large area nanoscale subcomponents.

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[8] RIE of SiO_2 was performed with $CHF_3/O_2/CF_4$ gas mixture (25/5/50 SCCM) and 50 W rf power.
[9] Certain commercial equipments or material suppliers are identified in this paper for describing experimental procedure adequately. This does not imply endorsement by NIST.
[10] Carrier concentration and resistivity data of *a*-Si as a function of diffusion temperature and time was generated by depositing *a*-Si on sapphire substrate and utilizing Hall effect and four-point resistivity measurements to characterize its electrical properties. The diffusion process with temperature ranging from 750 to 850 °C for 15 min resulted in *p*-doping density in *a*-Si in the range of 5×10^{19}–4×10^{20} cm^{-3} and hole mobility in the range of 5–2 $cm^2\ V^{-1}\ s^{-1}$. Diffusion time of 15 min resulted in a uniform dopant profile as confirmed by depth profiling, where resistivity was measured as the film was etched in regular steps. It is worth mentioning that after diffusion, XRD revealed the onset of crystallization in *a*-Si layer.
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