Realization of reliable GaN nanowire transistors utilizing dielectrophoretic alignment technique

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We have utilized dielectrophoretic force for assembling long (50 μm to 200 μm) GaN nanowires for device fabrication. These catalyst-free nanowires were grown by direct reaction of NH_3 and Ga, which resulted in free-standing nanowires along with GaN microplatelets. GaN nanowires were suspended in a solvent using sonication, and using dielectrophoretic forces nanowires were assembled on prepatterned substrates (SiO_2 coated Si and sapphire). With fabrication sequence using batch fabrication processes such as standard photolithography, etching, and oxide deposition we were able to realize stable GaN nanowire devices. The present technique is potentially compatible with complementary metal-oxide semicondoctor technology, and integrating nanodevices with conventional Si microelectronics on the same chip can be made possible with this technique. Utilizing this technique, high mobility (230 $cm^2\ V^{-1}\ s^{-1}$) GaN nanowire field effect transistors with reliable electrical characteristics have been achieved. These nanowire transistors even after prolonged period of conduction exhibited no deteriorations of their electrical properties. Several key factors in the processing that affect the device yield and reliability have been identified. Simple calculations predicted the effects of nanowire geometry, dispersing solvent, and alignment frequency on the dielectrophoretic force experienced by the nanowires. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2397383]

I. INTRODUCTION

Semiconducting nanowires and carbon nanotubes owe their unique properties to their reduced dimensionalities. Such nanoscale materials and structures can be used to realize electronic and optoelectronic devices and to study fundamental transport properties in mesoscopic systems.[1–5] The Group IIIA nitrides (binary and ternary alloys of AlN, GaN, and InN) have unique properties such as a direct band gap spanning the whole solar spectrum (from 0.7 eV for InN to 6.2 eV for AlN), high saturation velocity, and high breakdown electric field. As a result nanostructures and nanodevices made from GaN and related nitrides have great potential for realizing next generation efficient nanoscale UV/visible light emitters, detectors, and gas sensors. Successful integration of these nanowire devices (nanocomponents) with Si microelectronics will eventually lead to the multifunctional, complex nanosystems, e.g., multispectral emitter/detector, optical signal processors, and multicomponent gas sensors.

Results of individual GaN nanowire devices reported so far[4,6,7] utilize fabrication processes which require individual nanowire manipulation and registration to form metal contacts. These processes often involve time consuming serial techniques such as electron beam lithography, scanning probe techniques, and atomic force microscope manipulation. Such techniques are unsuitable for large scale batch fabrication. To this date, assembly of nanowires without individual registration has been attempted mainly using electric field assisted aligning,[3] chemical patterning, or microfluidic aligning.[8] Although simple assemblies have been obtained using these techniques, so far the most complex hierarchical nanowire network has been assembled utilizing the Langmuir-Blodgett (LB) technique.[9] Even though the LB

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technique is quite successful in creating dense networks of nanowires with repeatability and significant yield, it requires addition of surfactants to the nanowire suspension and complex compression procedures for the monolayer formations. This makes the LB process incompatible with the complementary metal-oxide semicondoctor (CMOS) processing technology.

We have utilized an electric field assisted alignment technique and a fabrication process sequence, which is compatible with Si very large scale integrated (VLSI) processing. Utilizing this technique we were able to form GaN nanowire devices with stable Ohmic contacts, embedded in an oxide passivation layer. A reliable GaN nanowire *n*-type depletion mode metal-oxide-semiconductor field effect transistor (MOSFET) has been achieved utilizing a Si substrate as the backgate. Effects of process parameters (annealing temperature, substrate type, and passivation layer thickness) on the device properties and yield have been identified.

II. THEORETICAL BACKGROUND

A neutral particle placed in a nonuniform electric field experiences a force due to the interaction of the induced dipole moment with the divergent electric field. This force is called the dielectrophoretic (DEP) force, and the translational motion of the neutral particle caused by this force is termed dielectrophoresis.[10] Aligning or manipulating particles using the dielectrophoretic force relies on the difference in polarizability of the particle and the medium used for suspending the particles. Generally the suspending medium is an organic solvent such as isopropanol (IPA), ethanol, acetone, etc. The force experienced by a neutral particle in such a solution due to the nonuniform electric field is given by the following relationship (bold faced letters indicate vector quantities):

$$\mathbf{F}_{\mathrm{DEP}}(t) = [\mathbf{p}(t) \,.\, \nabla]\mathbf{E}(t), \tag{1}$$

where $\mathbf{F}_{\mathrm{DEP}}(t)$ is the time dependent dielectrophoretic force experienced by the particle, $\mathbf{p}$ being the induced dielectric moment vector, and $\mathbf{E}(t)$ is the time varying applied electric field. The dipole moment vector, for the simple case where the body is isotropically, linearly, and homogenously polarizable, depends on the applied electric field as such

$$\mathbf{p}(t) = \alpha V \mathbf{E}(t), \tag{2}$$

where α is the polarizability tensor for the particle and V being total volume of the particle. It can be shown that the time averaged DEP force is given by the following equation:[11,12]

$$\langle \mathbf{F}_{\mathrm{DEP}} \rangle = \Gamma \varepsilon_m \,\mathrm{Re}\{k_f\} \nabla |\mathbf{E}_{\mathrm{rms}}|^2, \tag{3}$$

where Γ is the particle geometrical factor, $\mathrm{Re}\{k_f\}$ is the real part of the Clausius-Mossotti factor which depends on the shape of the particle, ε_m is the real part of the complex permittivity of the medium, and $\mathbf{E}_{\mathrm{rms}}$ is the root mean square value of the electrical field. The complex permittivity is given by

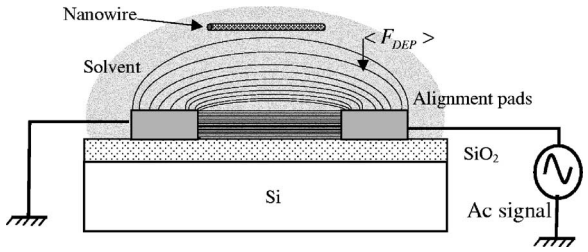


FIG. 1. Schematic representation of the dielectrophoretic alignment of nanowires using a solvent medium.

$$\varepsilon^* = \varepsilon - i\frac{\sigma}{\omega}. \tag{4}$$

The ε is the real permittivity, σ is the conductivity, and ω is the angular frequency of the applied electric field. For a cylindrical particle with length l and radius r where $l \gg 2r$, the k_f and Γ are given by

$$k_f = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^*}, \tag{5}$$

$$\Gamma = \frac{\pi}{6} r^2 l, \tag{6}$$

where ε_p^* and ε_m^* are the complex permitivities of the particle and the medium, respectively.

Figure 1 schematically explains the working principle of the dielectrophoretic alignment of the nanowires. When the nanowire suspension is dispersed on a sample with a voltage applied between two metal pads, the divergent electric field interacts with the induced electric dipole moment of the nanowire. The DEP force experienced by the nanowire is normal to the sample surface. In case of a positive dielectrophoretic force (determined by the difference in the dielectric permittivities of the nanowire and the dispersing medium) the nanowires will be attracted towards the pads and will eventually settle down on the pads with the complete evaporation of the solvent.

III. EXPERIMENTAL PROCEDURE

Although the proposed fabrication method can be used for nanowires of all possible material systems, we have demonstrated the effectiveness of this technique particularly by assembling long GaN nanowires on prepatterned substrates, forming device structures with a metal contact scheme suitable for the nitride material system. The GaN nanowires used for this study were grown by direct reaction of Ga and NH_3 and had diameters ranging from 50 nm to 300 nm and lengths up to 200 μm as reported elsewhere.[13] The growth results in the formation of the dense networks of GaN nanowires emerging from a thin layer of randomly oriented GaN microplatelets, which are deposited directly on the walls of the growth chamber. This growth assemblage will be referred to as the growth matrix from here on.

The growth matrix as collected from the growth chamber is sonicated in a solvent (isopropanol) using short ultrasound pulses to create a suspension of nanowires. Two different types of substrates were used to implement the assembly

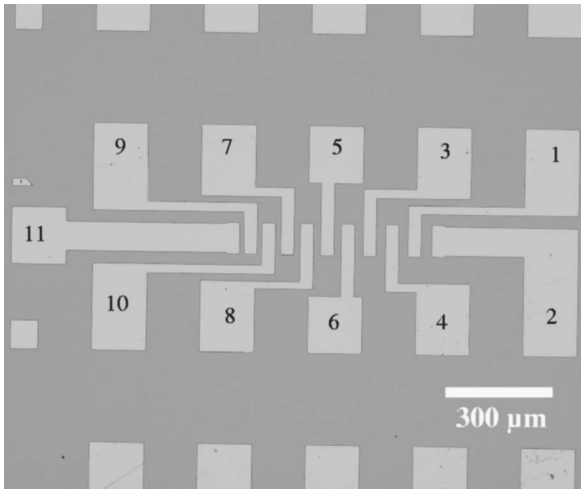


FIG. 2. Typical Ti/Al/Ti alignment pads on SiO_2/Si substrate. The spacings between the interdigitated electrodes varied from 14 μm at the one end (between electrodes 11 and 9) to 28 μm at the other end (between electrodes 2 and 1).

process: SiO_2 (600 nm, thermal oxide) coated Si substrates (n++, ρ=0.02 Ω cm, Silicon Quest International) (Ref. 14) and (0001) oriented sapphire substrates. The substrates were cut into 10×10 mm^2 pieces and were cleaned using standard Si cleaning procedure. Standard photolithography was carried out, followed by metal deposition Ti/Al/Ti (300 Å/1000 Å/300 Å) and lift-off. The final structure resulted in pads as seen in Fig. 2. These pads not only serve as alignment electrodes but they also act as bottom contacts for the nanowires. So it is necessary to select a metal scheme which is suitable for making Ohmic contacts to the nanowire material system. Forming Ohmic contacts to nitrides requires annealing at temperatures as high as 750 °C. For an n-type GaN, the Ti/Al/Ti/Au metal scheme has been proven to be low resistance and extremely reliable.[15] For the purpose of forming the bottom contact, Au is intentionally avoided from the metal stack, as otherwise the nanowire will be in direct contact with Au after bridging the alignment pads. Annealing the pads for Ohmic contact formation will form Au–GaN reaction products, which are proven to be detrimental to the contact properties.[16] Having both the bottom and top contacts for the nanowire devices not only ensures reliable device structures, but also enables us to estimate the material and contact properties more accurately.[17]

After the formation of the metal pads, the samples were coated with hexamethyldisilazane (HMDS) before dispersing the nanowires. This step ensures that the nanowires adhere to the oxide surface and not lift-off during subsequent processing. The nanowires are dispersed on the sample using Hamilton microliter syringes. For an alignment pad area of 650 $\times$1600 μm^2, 10 μ of the dispensing solution was used. The electric field alignment was performed in a regular probe station with 7 μm diameter W probes, and the solution dispensing syringe needle is placed right over the pad area. Voltage was applied to the end pads (2 and 11 as shown in the Fig. 2). The distance between the end pads (pads 2–11) is about 600 μm. The interdigitated alignment features have varying separation between them (from 14 μm at the one end to 28 μm at the other end). This arrangement ensures that the applied electric field is distributed between the pads according to the spacing between the gaps, and under no circumstances the nanowires can bridge the two extreme voltage probes. This will prevent the nanowires from being damaged by large current flows. A 20 V peak-peak ac voltage is applied during the alignment, between pad 2 and pad 11. The voltage is applied until the solvent dries out. The alignment is carried out on different regions of the samples to obtain multiple devices on the same substrate.

After the alignment is complete, the sample is cleaned using oxygen plasma (25% O_2 in argon, 20 mTorr, 50 W, and 1 min) to clean organic residue left after the evaporation of the solvent. The sample is then annealed using a rapid thermal annealer at 500 °C for 30 s in ultrahigh purity argon (first step anneal). This annealing step ensures that the contacts between the nanowires and the alignment pads are mechanically stable. Using plasma enhanced chemical vapor deposition technique, 30 nm to 100 nm of SiO_2 is deposited on the sample with the deposition temperature kept at 300 °C. After the oxide deposition, a second photolithography was performed to align the same pattern on the sample. Etching the oxide through the photoresist mask in buffered HF etching solution is performed to open the windows right over the preexisting alignment metal pads. A metal deposition was followed with a lift-off in acetone. The deposition sequence is Ti/Al/Ti/Au (300/1000/300/300 Å) with Au being the topmost layer. The sample is then annealed at ultrahigh purity (uhp) Ar at 750 °C for 30 s (second step anneal). The complete fabrication process is shown schematically in Fig. 3. This process results in the robust nanowire device structures, which are embedded in a protective plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer. This oxide can be removed for specific device applications such as sensor arrays or detectors, etc. Without the oxide coating, some nanowires were detached from the substrate during the lift-off for the second metal pad. The yield of the nanowire devices with the PECVD oxide coating was close to 80%.

Electrical measurements of the nanowires have been performed using a Keithley 6430 subfemtoamp source measure unit with remote preamplifier. All the electrical measurements are performed in a dark enclosure with a cable guard extended to the device under test (DUT). Multiple devices have been tested on each sample before and after annealing.

After completing electrical characterizations, the nanowire devices are examined utilizing a Hitachi S-4700 field emission scanning electron microscope (FESEM) to correlate their electrical properties with their structural characteristics.

IV. RESULTS, CALCUATIONS, AND DISCUSSION

The GaN matrix with attached nanowires as collected from the growth chamber is shown in the FESEM image in Fig. 4(a). This matrix consists primarily of two distinct features, viz., single-crystalline GaN nanowires and GaN platelets. The diameters of these platelets range from 0.5 μm up to 5 μm, and it has been confirmed by electron beam backscat-

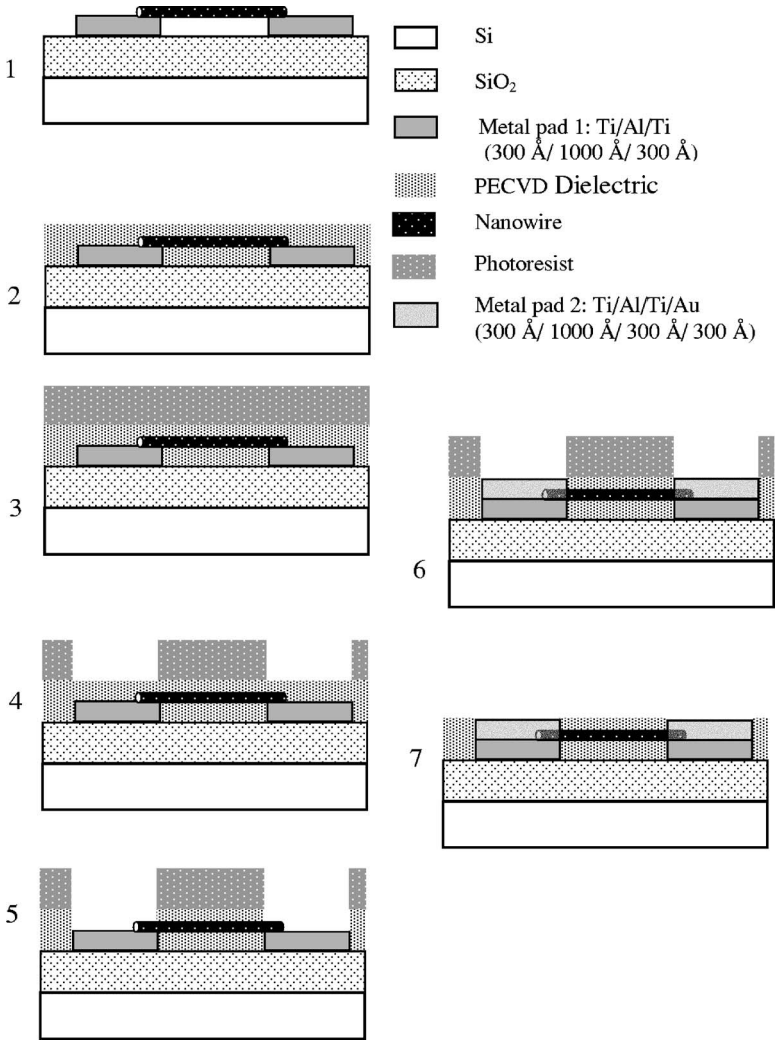
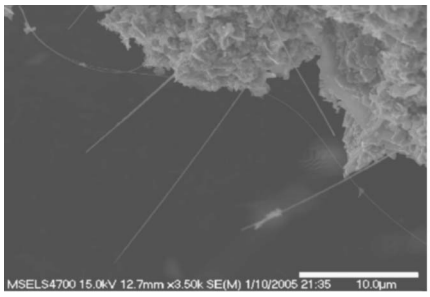


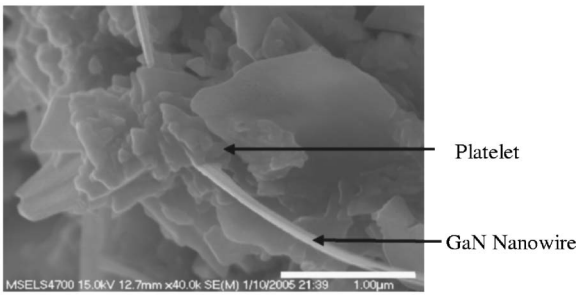
FIG. 3. Schematic representation of the fabrication process flow.

tered diffraction (EBSD) technique that the normal to these GaN platelets is the *c* axis of the wurtzite structure. From Fig. 4(b) it appears that the nanowires grow from the side facets of GaN platelets, which corresponds to the *a* planes of the wurtzite structure. Thus the nanowire axis was also in the *a* direction as confirmed by EBSD.[18]

The yield of the alignment and device properties are directly related to the nature of the dispersion. To understand the nature of the dispersion, it is important to study the statistical distribution of the diameters and structural nature of the nanowires in a growth matrix. A low resistivity Si sample was prepared with nanowires dispersed on it. Using FESEM, the diameters of 100 nanowires were measured at different parts of the sample. Figure 5 is the diameter distribution as observed on the growth matrix used for this study. It is quite clear that majority of the nanowires had diameters in the range of 50 nm to 100 nm. Only few nanowires were observed with diameters in excess of 200 nm. It was interesting to note that the structural quality of the nanowires showed significant variations with their diameters. As shown in Fig. 6(a), the nanowires with diameters in the range of 50 nm to 100 nm had circular cross sections with no observable defects. For nanowires with diameters above 150 nm [Fig. 6(b)], the defects in their structure are clearly visible in SEM scans. Larger diameter nanowires [Fig. 6(c)] repre-



(a)



(b)

FIG. 4. (a) FESEM scans of the growth matrix after collecting from the growth chamber. (b) FESEM scans of nanowires growing from the edges of the GaN platelets.

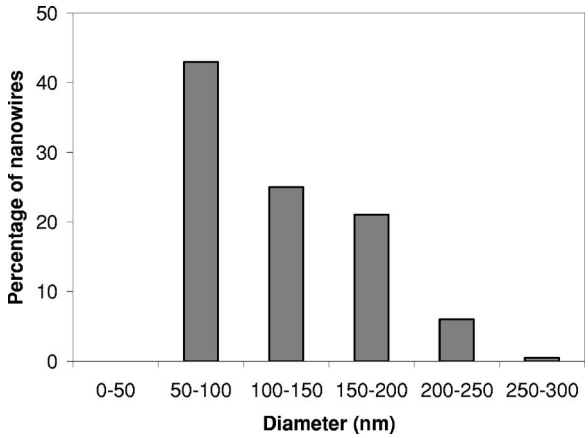


FIG. 5. Diameter distribution of nanowires as observed in the growth matrix.

sented a bundle of several crystals featuring similar growth direction and grown together so that the intercrystal boundaries were parallel to the wire axis. The complex crystallography exhibited by these multiple crystal assemblages within the individual nanowires is a subject of a continuing investigation.

Figure 7 is the FESEM scan of aligned nanowires utilizing a 1 kHz, 20 V peak-peak ac signal applied between the pads 2 and, 11 (see Fig. 2). The best possible alignment is obtained utilizing a 1 kHz alignment frequency. It will be shown later that this agrees well with the theoretical calculations. Generally only one or two wires tend to be present per alignment gap. As the DEP field strength reduces after a nanowire is captured between the alignment pads, other nanowires are no longer attracted towards the same gap. Thus engineering the alignment gaps to capture and manipulate a single nanowire is essential for developing complex architectures. After the dispersing solvent dries out, the nanowires tend to adhere to the metal pads. The van der Waals force is likely responsible for the attraction between the nanowires and the metal pads after the solvent dries out. Even gentle cleaning of the samples in solvents does not lift-off the aligned nanowires. Although the aligned nanowires adhere to the metal alignment pads, it was observed in SEM that the nanowires were not laying flat on the metal

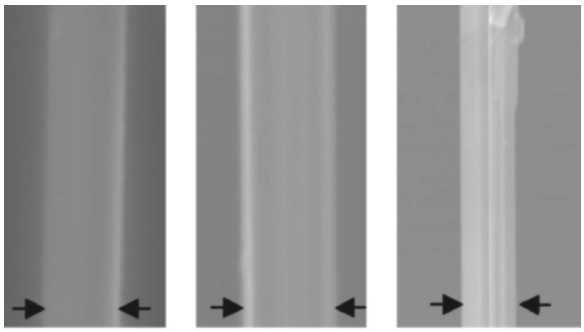
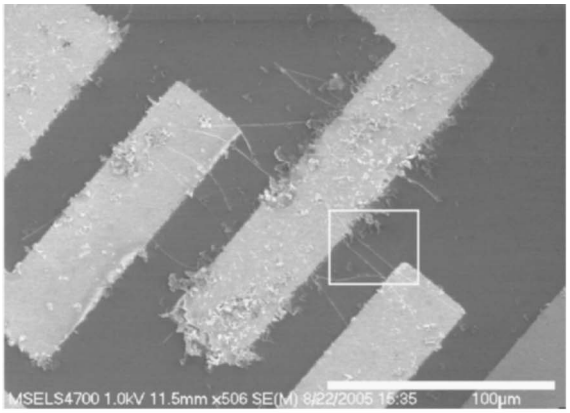
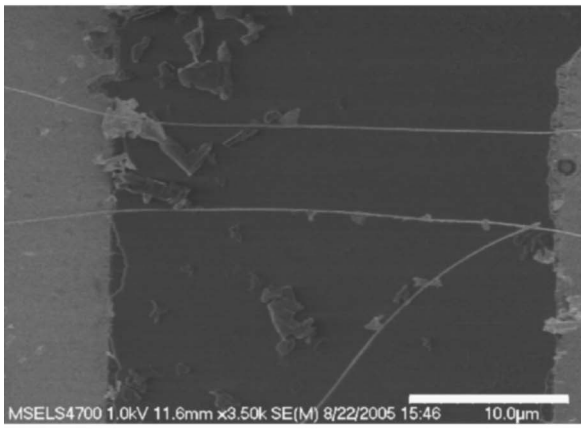


FIG. 6. Representative structural characteristics of nanowires observed in different diameter ranges: (a) 50–100 nm, (b) 150–200 nm, and (c) 250–300 nm. Diameters of the nanowires are indicated below.



(a)



(b)

FIG. 7. FESEM images of GaN nanowires aligned on Ti/Al/Ti pads using DEP force. (a) Nanowires aligned using a 1 kHz 20 V peak-peak ac signal. (b) Magnified image of the area surrounded in (a) with the white box.

pads and on the substrate, hence they do not make stable mechanical contacts. Electrical measurements performed on the alignment pads with nanowires between them showed that the contacts are unstable and in most cases nonconductive. Even after annealing the samples with nanowires between the alignment pads at 500 °C for 30 s the bottom contact pads do not form reliable contacts to the nanowires. After depositing the second metal stack (Ti/Al/Ti/Au), *I-V* characteristics were measured on the samples. Almost 70% of the nanowires had linear Ohmic contacts, with high current levels (in the range of 10^{-6} A to 10^{-5} A for 0.5 V bias). Figure 8 shows the current-voltage characteristics of such a nanowire with the as-deposited second metal stack and after annealing the second metal stack at 750 °C for 30 s. These nanowires with linear *I-V* characteristics showed negligible or no improvement in their *I-V* characteristics after annealing as evident from the plot (Fig. 8). While for some of the nanowires, the as-deposited contact properties were nonlinear with low current levels (in the range of 10^{-11} A to 10^{-9} A for 0.5 V bias) as seen in Fig. 9(a). The nanowires which exhibited lower current levels with nonlinear *I-V* characteristics also showed only marginal improvements. In some cases, nanowires with a low current level before annealing showed improvements after annealing [Figs. 9(a) and 9(b)], but the current level did not increase to

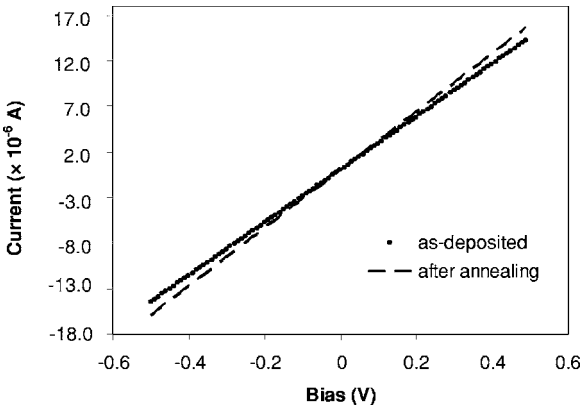


FIG. 8. *I-V* characteristics of a single nanowire (100 nm diameter and 35 μm in length) with the as-deposited second metal stack (*) and after annealing (--).

the 10^{-6} A to 10^{-5} A range as observed in majority of other devices. In order to investigate the physical factors responsible for the electrical behavior of the nanowires, we used FESEM to scan the nanowires for which we have already measured the *I-V* characteristics. We found that nanowires with linear *I-V* characteristics and high current levels had perfect contacts at the both ends, whereas nanowires with low current levels either had insufficient contact coverages (contacts did not bridge the nanowire completely) or they

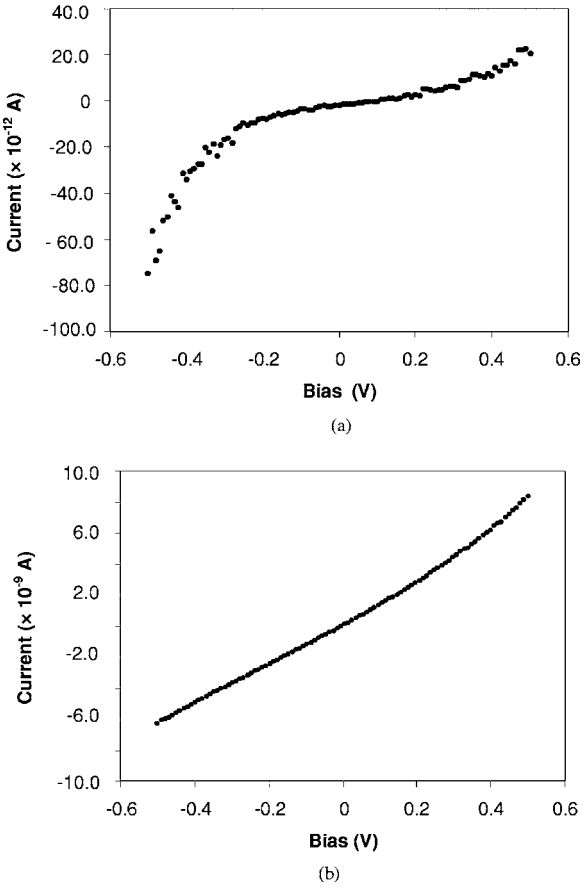


FIG. 9. (a) *I-V* characteristics of a nanowire with the as-deposited second metal stack showing nonlinear behavior with the lower current levels. (b) *I-V* characteristics of the same nanowire after annealing the second metal stack.

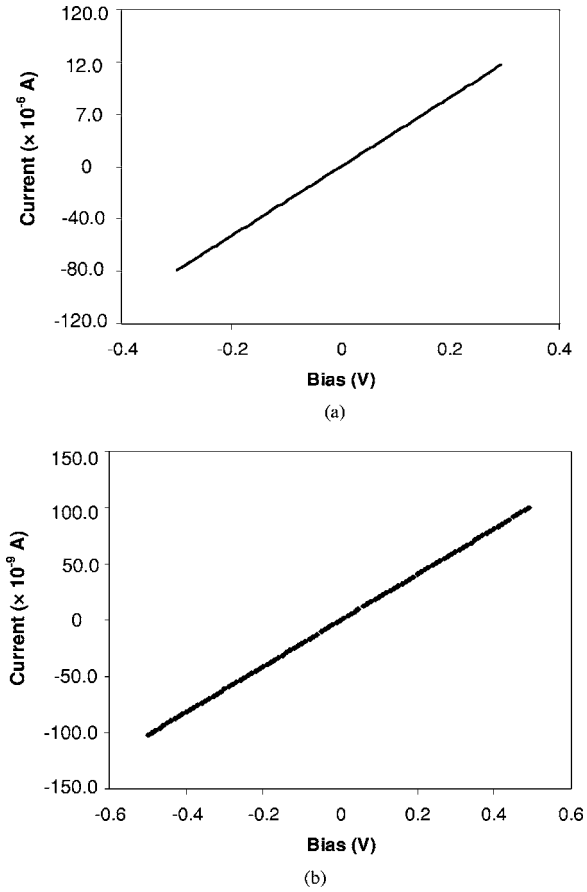


FIG. 10. (a) *I-V* characteristics of a single nanowire (110 nm diameter and 30 μm in length) with the as-deposited second metal stack. (b) *I-V* characteristics of the same nanowire after annealing the second metal stack showing significant deterioration.

had structural damages. There are also instances where the nanowire with as-deposited second metal stack had liner a *I-V* characteristics before annealing, but after annealing degradations in the *I-V* characteristics were noted [Figs. 10(a) and 10(b)]. Investigating with FESEM revealed that these nanowires developed structural damage after annealing. Figure 11 is the FESEM scan of the nanowire (*I-V* characteristics of this nanowire is presented in Fig. 10) between two pads on a sapphire substrate after annealing. PECVD oxide is absent in this sample. The stress that developed between the pads during annealing may have caused structural damage to the nanowires. This type of deterioration was less common in PECVD oxide coated samples. Over many devices it was observed that samples with a PECVD oxide thickness greater than 30 nm had higher yield, than samples with thinner oxide. It was also generally found that nanowire devices assembled on a SiO_2/Si substrate had better yield than on sapphire substrates. Unlike the case of thin-film GaN devices, annealing the contacts to the nanowires only marginally improved their electrical properties. It is important to optimize the annealing temperature and heating rate to reduce thermal stresses during annealing.

Nanowire channel current modulation has been achieved by applying bias to the Si substrate with Al deposited on the backside for contact formation. As expected, a depletion mode behavior with *n*-type conductivity is observed in all

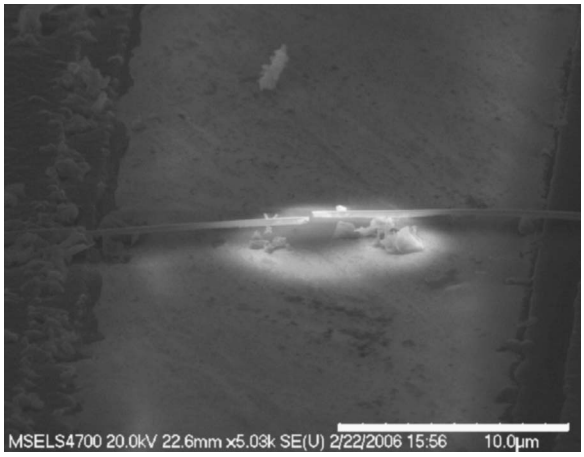


FIG. 11. FESEM scan of the nanowire device (*I-V* characteristics present in Fig. 10) after annealing of the second metal stack. The break in the nanowire is clearly visible, which might be caused by the thermal stress during annealing. This nanowire is assembled on a sapphire substrate with no PECVD protective oxide coating.

devices. The presence of lattice defects and contaminants such as oxygen is likely a source of *n*-type background concentrations often found in these types of growth methods. Detailed electrical characterizations over many devices revealed a general trend. Majority of the nanowire FETs (termed type I) showed no pinch-off characteristics, with high drain-source current (I_{DS}) levels in the range of 10^{-6} A to 10^{-5} A for 1 V drain-source voltage (V_{DS}) and 0 V gate-source voltage (V_{GS}). Figure 12(a) shows the plot of I_{DS} vs V_{DS} for a nanowire device of type I (diameter of 200 nm and length of 44 μm) with V_{GS} varied from −40 V to +40 V. For these types of devices, the channel current does not saturate even at high values of V_{DS} (±4 V). From the transconductance curve (I_{DS} vs V_{GS} plot) in Fig. 12(b), the electron field effect mobility (μ) is calculated using the following relationship:[8]

$$\mu = \frac{g_m}{V_{DS}} \frac{L \ln(4t_{ox}/d)}{2\pi\varepsilon_0\varepsilon_{SiO_2}}, \tag{7}$$

where the transconductance (g_m) is the slope $\partial I_{DS}/\partial V_{GS}$ calculated from the I_{DS} vs V_{GS} plot, L and d are the length and diameter of the nanowire, respectively, t_{ox} is the oxide thickness (600 nnm), ε_0 is the permittivity of free space, and ε_{SiO_2} is the permittivity of the silicon dioxide. The calculated mobility for this particular device (diameter of 200 nm and length of 44 μm) was 230 $cm^2\ V^{-1}\ s^{-1}$, which is significantly higher (by an order of magnitude) than the majority of the results published so far.[6,19,20] Mobilities in this range were found in majority of our devices. A report on GaN nanowire FET mobilities higher than the present result is by Huang *et al.*, where they reported mobilities in the range of 640 and 300 $cm^2\ V^{-1}\ s^{-1}$ in a batch of ten devices.

Other types of device (type II) had lower current levels (10^{-7} A to 10^{-6} A for 1 V V_{DS}), and showed complete channel depletion from −40 to −30 V V_{GS} with an on-off current ratio of about 10^7. FESEM revealed that these devices had diameters about 100 nm and less. Figure 13(a) shows the plot I_{DS} vs V_{DS} of a nanowire device of type II (diameter

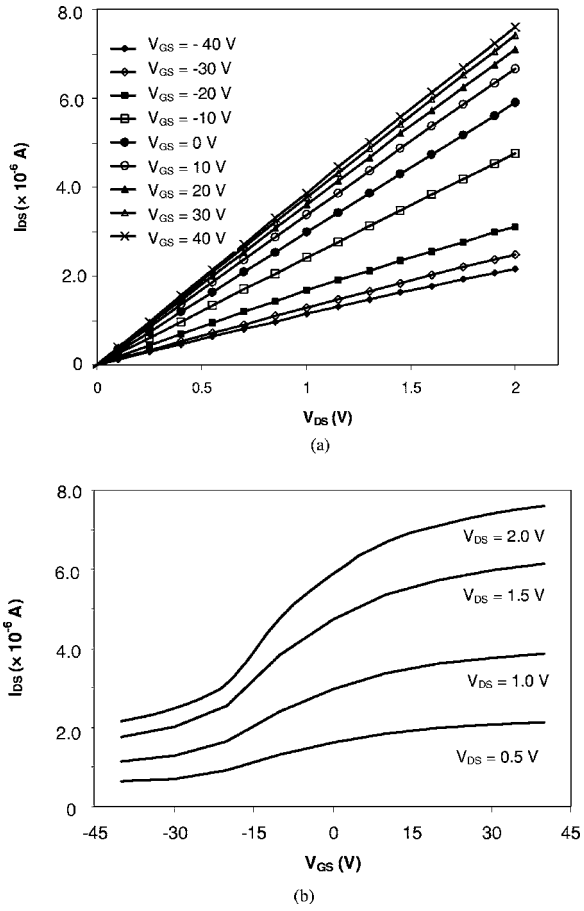


FIG. 12. (a) I_{DS} of vs V_{DS} plot for a nanowire device of type I (diameter of 200 nm and length of 44 μm) with V_{GS} varied from −40 to +40 V. (b) Transconductance plot of the same nanowire device (I_{DS} vs V_{GS}) for different V_{DS}.

of 95 nm and length of 35 μm) with V_{GS} varied from −30 V to +40 V. The mobility of this device [calculated using Eq. (7) and Fig. 13(b)] was 40 $cm^2\ V^{-1}\ s^{-1}$. It was interesting to note that the mobility values of smaller diameter nanowires were less than the larger diameter nanowires. The lower mobility in smaller diameter nanowires might be caused by surface scattering. Detailed analysis has to be carried out to understand the role of surface scattering in electron transport through these nanowires.

Electrical characterization and FESEM scans revealed that majority of aligned nanowires had diameters in range of 150 nm to 200 nm. This is surprising given the fact that the diameter distribution study (Fig. 5) showed that majority of nanowires in the dispersion had diameters in the range of 50 nm to 100 nm. In order to understand the effects of nanowire dimensions, dispersing medium, and frequency of the aligning voltage on the DEP forces experienced by the nanowires, detailed calculations have been performed using a simplified model. The physical situation of the nanowires dispersed in a solvent can be modeled assuming that the nanowires are perfectly cylindrical particles (with $l \gg 2r$). Using (3)–(6), we have calculated the relative DEP forces experienced by a GaN nanowire in the presence of different dispersing media. The real part of the Clausius-Mossotti factor for a cylindrical particle from (5) is

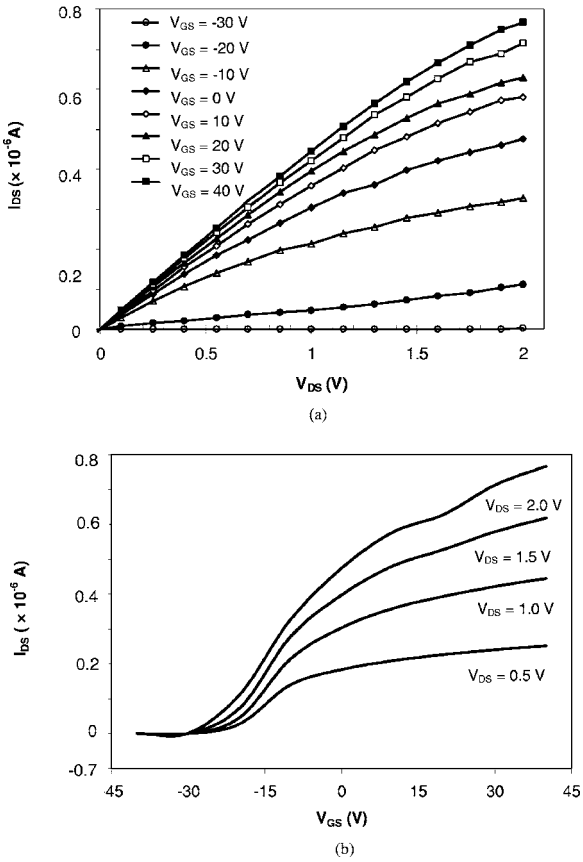


FIG. 13. (Color online) (a) Plot of I_{DS} vs V_{DS} of a nanowire device of type II (diameter of 95 nm and length of 35 μm) with V_{GS} varied from −30 to +40 V. (b) Transconductance plot of the same nanowire device (I_{DS} vs V_{GS}) for different V_{DS}. The device could be completely turned off at −30 V V_{GS}.

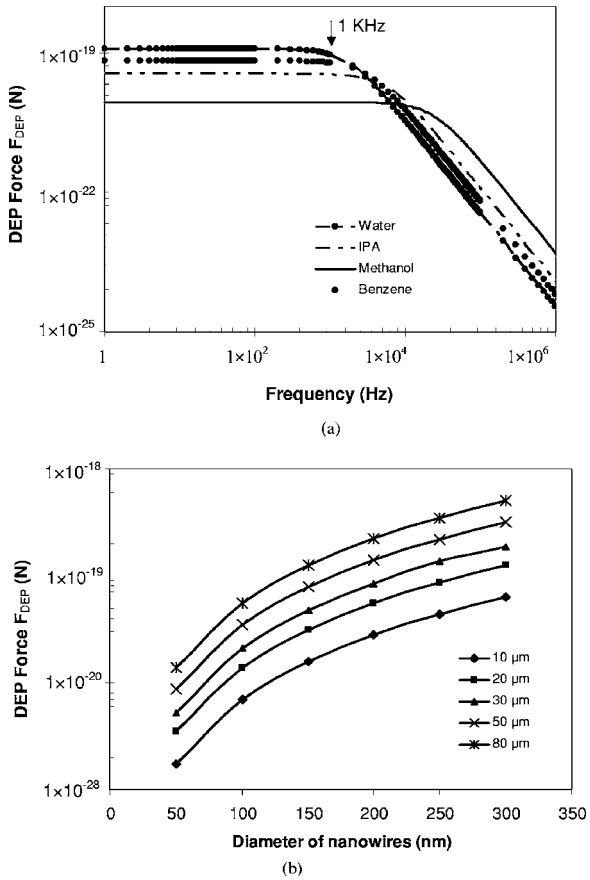


FIG. 14. (a) Calculated DEP force experience by a nanowire (100 nm diameter and 50 μm in length) in different dispersing media as a function of the alignment voltage. The drop in the DEP force for different solvents starts around 1 kHz. (b) Calculated DEP force variation as a function of nanowire diameter and length. The alignment frequency is set to 1 kHz and the dispersing medium is IPA.

$$\mathrm{Re}\{k_f\} = \frac{\omega^2 \varepsilon_m(\varepsilon_p - \varepsilon_m) - \sigma_m(\sigma_m - \sigma_p)}{\omega^2 {\varepsilon_m}^2 + {\sigma_m}^2}. \tag{8}$$

Figure 14(a) shows the relative dielectrophoretic force variations for a 100 nm radius and 50 μm long nanowire dispersed in water, isopropanol, ethanol, and benzene as a function of the bias frequency. Table I lists all the parameters used for calculating the relative dielectrophoretic forces for a nanowire in different solvents. For comparison purposes all the calculations were performed assuming unit $\nabla|\mathbf{E}_{\mathrm{rms}}|^2$. The conductivity of the nanowires used for the calculations was experimentally obtained to be around $2.0\times10^4\ \Omega^{-1}\ \mathrm{m}^{-1}$.[18] The relative dielectric permittivity for GaN used for the calculation was 9.70. From Fig. 14(a) it is clear that at low frequencies, between 1 Hz and 1 kHz, the DEP force is constant with the frequency for different dispersions. From Eq. (8) it can be seen that at low frequencies the DEP force is determined by the difference in the conductivities of the particle and the dispersing medium, whereas at high frequencies the DEP force is proportional to the difference in their conductivities. Water, although having the largest DEP force factors out of the four dispersing media, is not a good choice for DEP alignment, as maintaining high resistivities, and low ionic conduction is challenging for water. Benzene appears to be an easier alternative to water with its DEP force factor comparable to water. Above 1 kHz, all the curves for different dispersing media experience a roll off associated with the dielectric relaxation of the medium and the particle. This agrees perfectly well with experimentally observed results, where the highest alignment yield was observed at 1 kHz alignment frequency.

Figure 14(b) is a plot showing the DEP forces experienced by nanowires in IPA as a function of their diameters for different lengths of the nanowires. The alignment frequency is 1 kHz with a peak to peak voltage of 20 V. It can be seen that thicker nanowires experience a larger DEP force than thinner nanowires. Thus nanowires with larger diameters will have a higher probability of alignment than nanowires with smaller diameters. This would explain the higher

TABLE I. Physical parameters used for the calculation of DEP forces for nanowire in different solvents.

Medium	Relative dielectric constant $\varepsilon_m/\varepsilon_0$[a]	Conductivity σ (S m^{-1})
Water	80.0	7.6×10^{-6}
Methanol	32.9	4.4×10^{-5}
Isopropanol	18.6	6.0×10^{-5}
Benzene	2.3	4.0×10^{-7}

[a]ε_0 denotes the dielectric constant of vacuum$=8.854\times10^{-12}$ F m^{-1}.

number of large diameter aligned nanowires (200 nm) even though the dispersion contains a higher number of nanowires with 100 nm diameters. Also there is about a one order of magnitude increase of the DEP force with the increase in length of the nanowires from 10 μm to 80 μm. This variation in DEP forces experienced by nanowires of different dimensions can be utilized for the selective alignment of nanowires.

V. CONCLUSION

We have been able to realize reliable, high performance GaN nanowire devices using a dielectrophoretic alignment technique. A simple fabrication process using only batch fabrication techniques is presented, which resulted in stable device characteristics. It was observed that annealing the metal contacts to the GaN nanowires only marginally improved their characteristics. Field effect transistor measurements revealed an *n*-type depletion mode behavior with mobilities as high as 230 $cm^2 V^{-1} s^{-1}$. Surface scattering seems to have a dominant effect on charge transport in smaller diameter nanowires. Using a simple model, it was shown that larger diameter nanowires experience larger dielectrophoretic forces than nanowires with smaller diameters. Calculations also predicted the suitable frequency range and solvents to maximize the alignment yield.

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