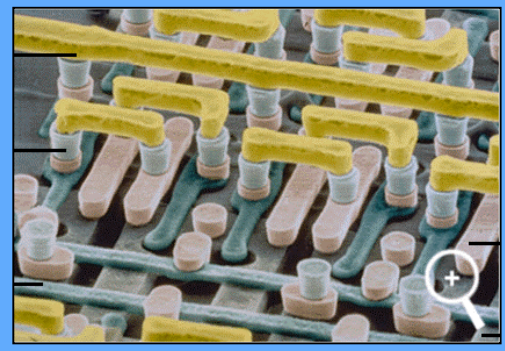
Novel Barrier Materials for Interconnect Applications

presented by D. Josell

February 7, 2006

Interconnects

Local level interconnects are less than 100 nm wide and getting thinner, with industry continuing to reduce the footprint of the transistors on the silicon wafer.


IBM

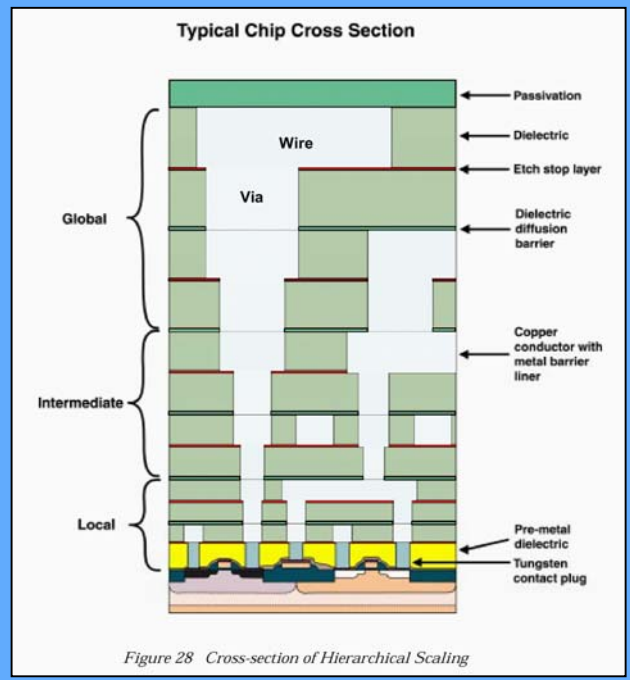


Figure 28 Cross-section of Hierarchical Scaling

Interconnects

International Technology Roadmap for Semiconductors 2004 update

Wiring *Pitch*

Year of Production	**2010**	**2013**	**2016**
Local (nm)	**108**	**76**	**54**
Intermediate (nm)	135	**95**	**65**
Global (nm)	205	140	**100**

No known solution

Manufacturable solutions are known

"In assessing the roadmap as a whole, however, it still becomes almost entirely "red bricks" by the end of this decade…"

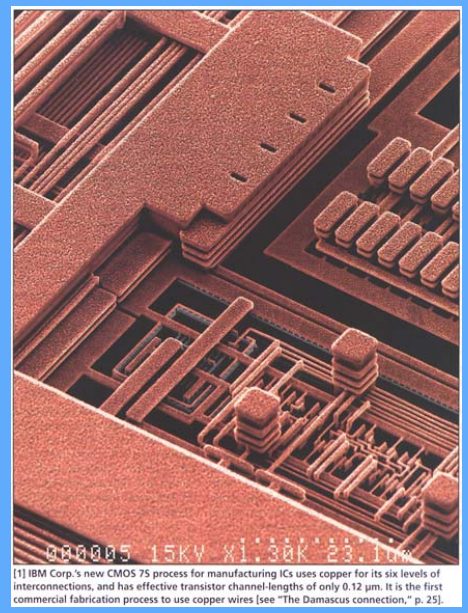
International Technology Roadmap for Semiconductors 2004 Update

NIST

Superfill for Cu Damascene Inteconnects

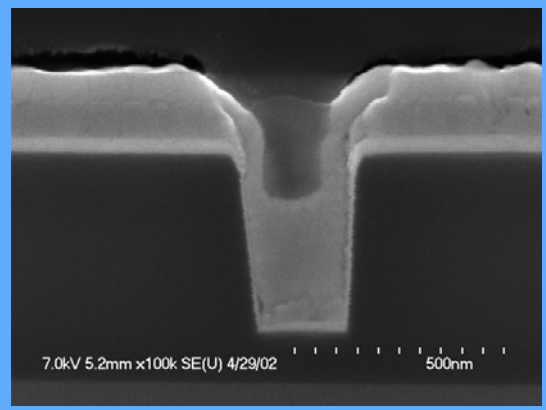
Bottom-up copper “superfill” through electrodeposition is used to fabricate state-of-the art interconnects for Si technology.

Diffusion barriers of Ta, TaN and/or TiN separate the Cu conductor from the surrounding dielectric.



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].

IBM



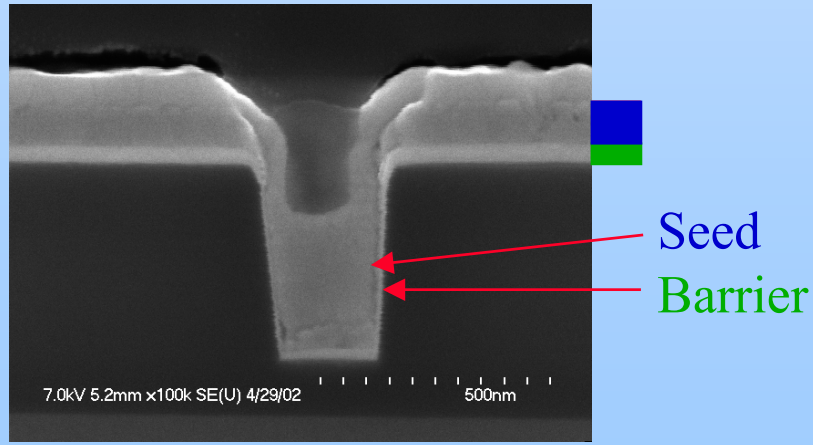
Bottom-up superfill

Challenge 1: Seed Fabrication

Fabrication of defect-free Cu seeds required for Cu electrodeposition on conventional diffusion barriers is becoming more difficult as features become smaller and narrower.

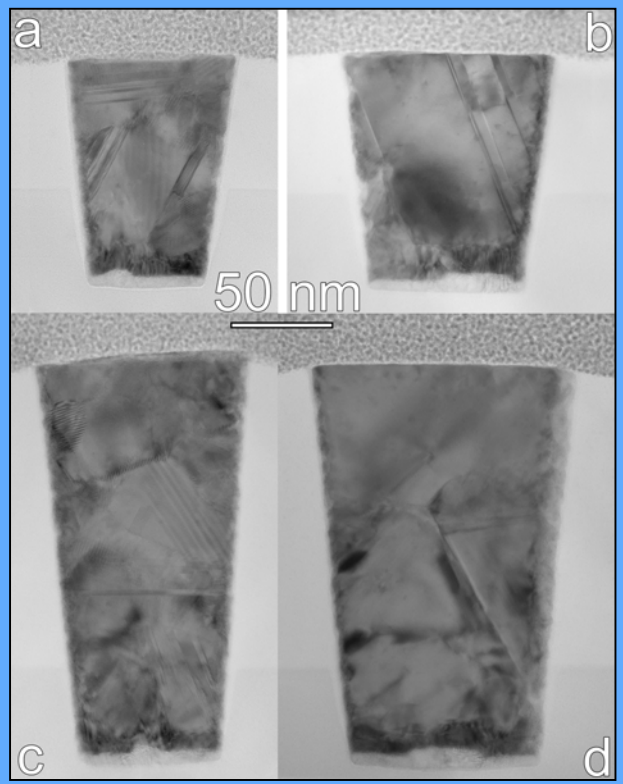
"*A more elegant solution to the problem … barrier to be self-nucleating thereby eliminating the need for a Cu nucleation layer.*"

ITRS 2003, Interconnects



Challenge 2: Size Effects

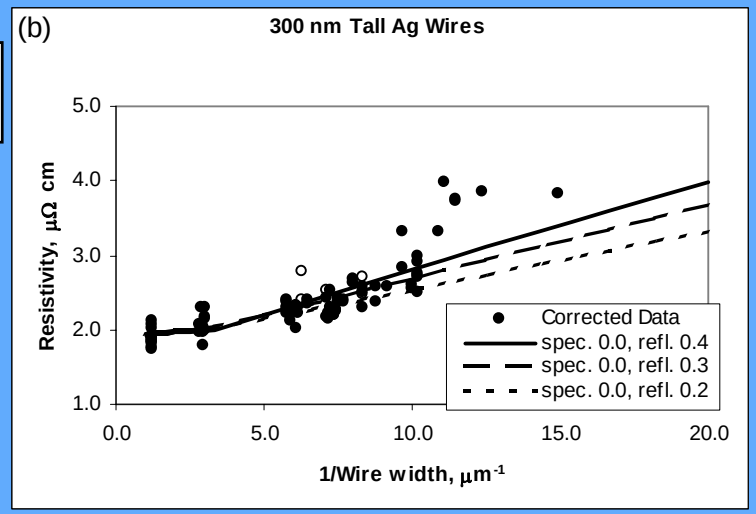
Electron scattering at the conductor/barrier interface and grain boundaries increase the resistivity of sub-100 nm interconnects. Thick, resistive barriers aggravate this.



Ag wires

J.E. Bonevich

Wire width, μm	Resistivity ρ_s, μΩ cm	Intrinsic, μΩ cm	Surface, μΩ cm	Grain boundary, μΩ cm
0.05	3.669	1.6	0.973	1.096
0.07	3.112	1.6	0.722	0.790



NIST

D. Josell, C. Burkhard, D. Kelley, Y.-W. Cheng, R.R. Keller, J.E. Bonevich, Y. Li, B.C. Baker, C.A. Witt, T.P. Moffat, J. Appl. Phys. 96(1), 759-768 (2004).

Interconnect Challenges

"Top three challenges

Introduction of new materials to meet conductivity requirements…

Mitigate impact of size effects in interconnect structures.

...

Defining and finding solutions beyond copper and low κ will require materials innovation… and unconventional interconnect."

ITRS 2004 Update

Novel Barriers

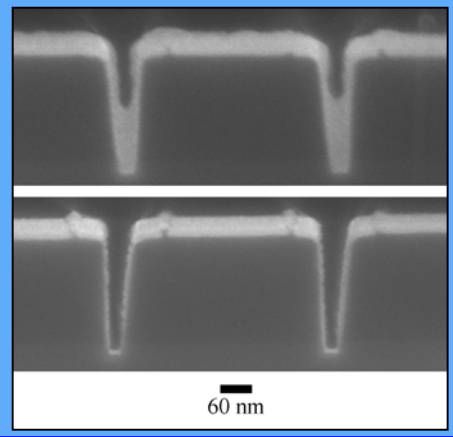
How about a new barrier material: one that has a lower resistivity than existing barrier materials like Ta and also permits direct Cu electrodeposition and superfill without the need for a Cu seed layer.

M.W. Lane suggested: Cu, Pt, Pd, Ru, Rh, Ir and Ag on the basis of enthalpy of formation of the barrier oxide as compared to that of copper oxide (Appl. Phys. Lett. 2003)

Ruthenium Barriers

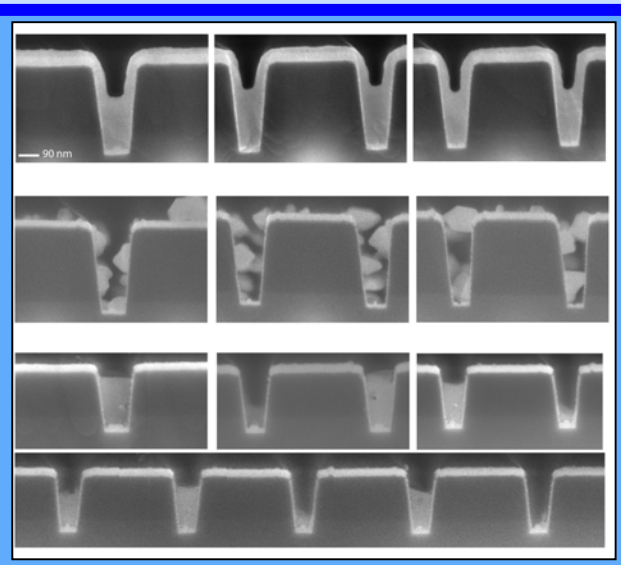
Seedless Cu superfill (on Ru).

D. Josell, D. Wheeler, C. Witt and T.P. Moffat, Electrochem. Solid-State Lett. 6(10), C143-C145 (2003).



Control wettability of Ru barriers.

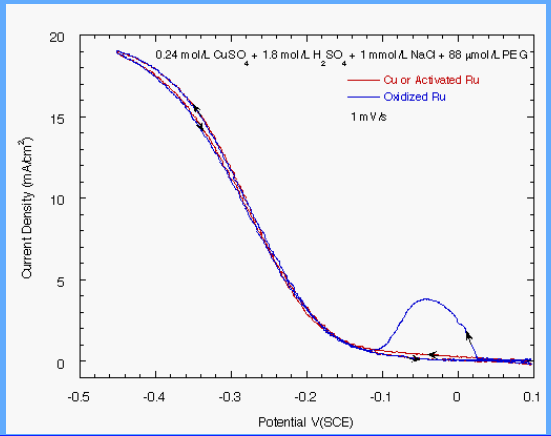
T.P. Moffat, M. Walker, P.J. Chen, J.E. Bonevich, W.F. Egelhoff, L. Richter, D. Josell, C. Witt, T. Aaltonen, M. Ritala and M. Leskelä, J. Electrochem. Soc. 153, C37 (2006).



Ruthenium Barriers

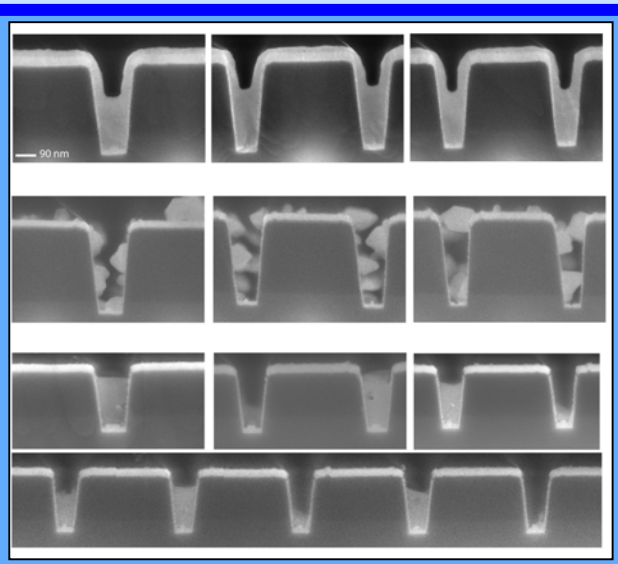
Current-voltage behavior can be used to assess the state of the Ru surface as a result of various activation processes.

T.P. Moffat and D. Josell, in Semiconductor FabTech 27th Edition, 133-136 (2005).



Process based on hydrogen reduction of surface oxide.(Moffat, ECS, Spring 2005).

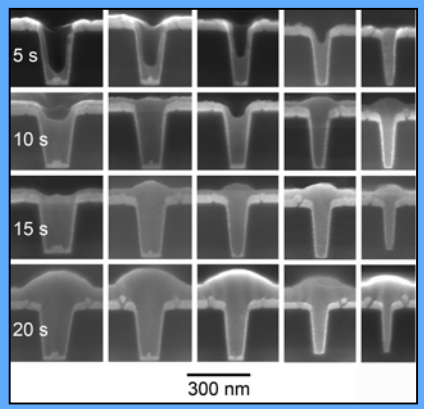
T.P. Moffat, M. Walker, P.J. Chen, J.E. Bonevich, W.F. Egelhoff, L. Richter, D. Josell, C. Witt, T. Aaltonen, M. Ritala and M. Leskelä, J. Electrochem. Soc. 153, C37 (2006).

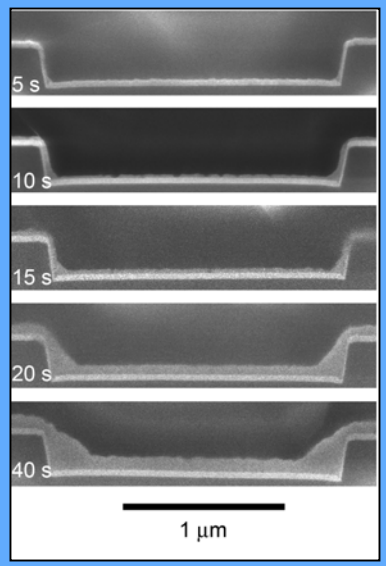


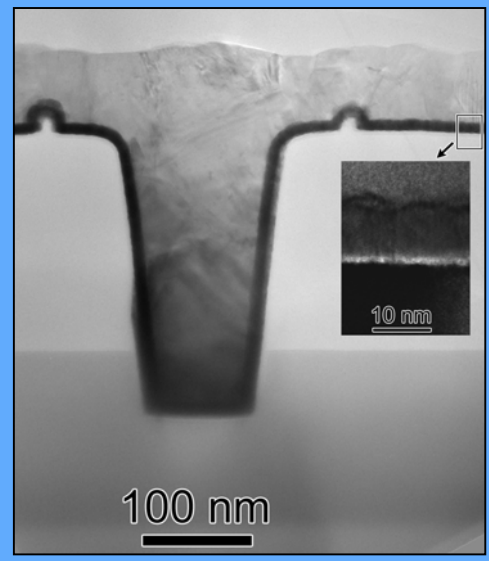
Other Barriers and Processes

Other barrier ***materials*** for seedless Cu superfill.

Osmium has a melting point over 3000 °C and negligible solubility with Copper.







J.E. Bonevich

New ***fabrication techniques*** like **atomic layer deposition** (ALD) for extremely thin and uniform barriers.

D. Josell, C. Witt and T.P. Moffat, Electrochemical and Solid-State Letters 9, C41 (2006).

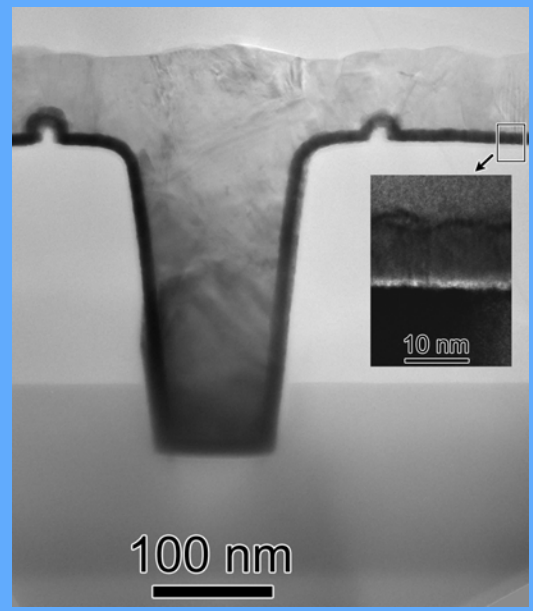
D. Josell, J.E. Bonevich, T.P. Moffat, T. Aaltonen, M. Ritala and M. Leskelä, Electrochemical and Solid-State Letters 9, C48 (2006).

ALD Iridium Barriers

10 to 15 nm thick Ir barriers were obtained using 200 or 300 cycles of an ALD process based on $Ir(acac)_3$ -- (2,4-pentanedionato)iridium -- and oxygen.

Iridium adhesion to the TEOS substrate material was promoted using several nm's of alumina deposited using an ALD process based on trimethyl aluminum and water.

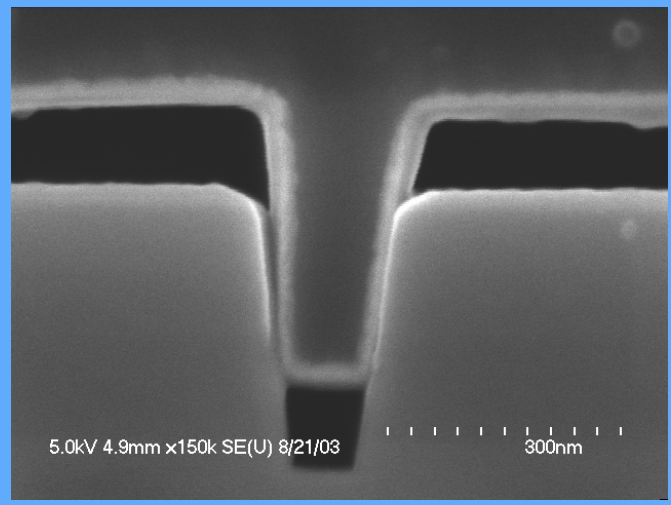
Aaltonen et al., J. Electrochem. Soc. **151**, G489 (2004).



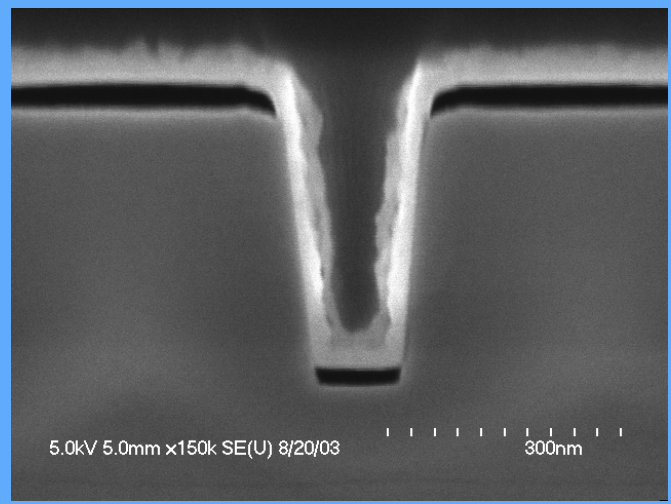
D. Josell, J.E. Bonevich, T.P. Moffat, T. Aaltonen, M. Ritala and M. Leskelä, Electrochemical and Solid-State Letters 9, C48 (2006).

ALD Iridium Barriers

Adhesion of ALD Ir barrier to the TEOS dielectric was poor absent the alumina adhesion layer.



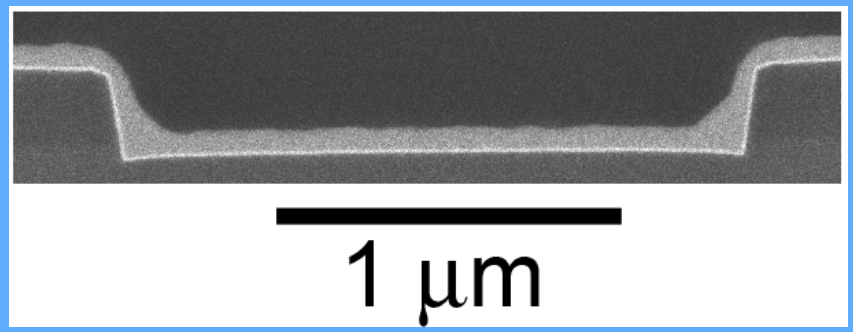
Adhesion of ALD Ru barrier to the TEOS dielectric was poor with an intervening water pulse (meant to create hydroxyl bonds) rather than the alumina adhesion layer.



NIST

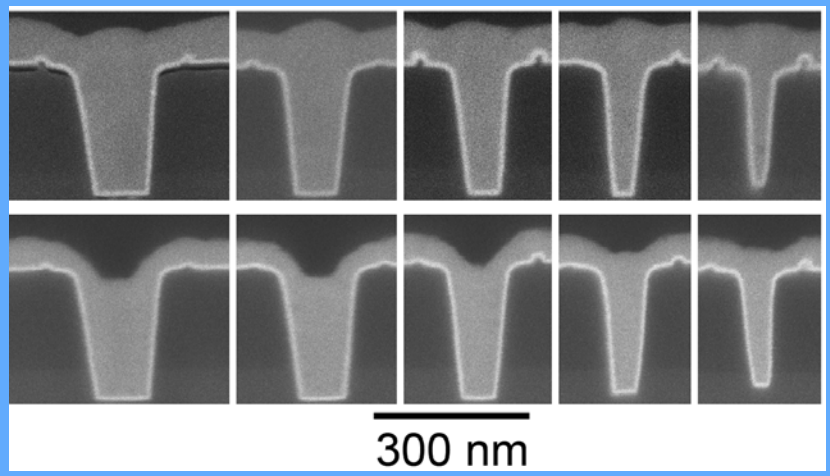
ALD Iridium Barriers

Cu deposition on ALD Ir barriers exhibits bottom-up filling geometry characteristic of superfill on Cu seed layers.

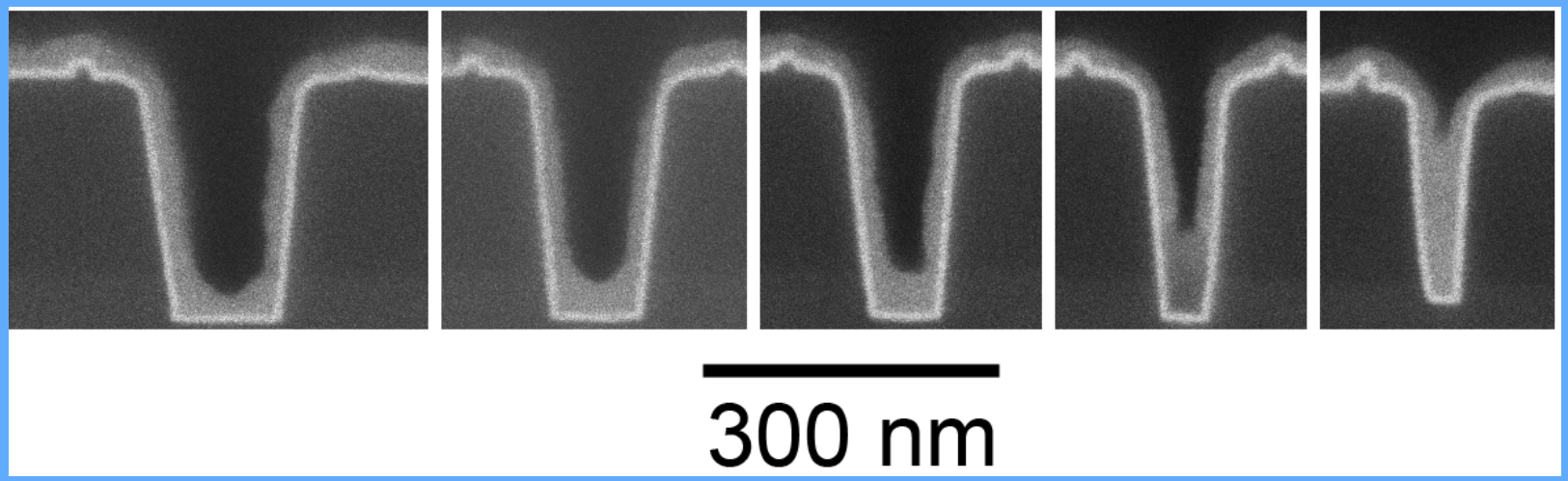


30 s at 0.1 V SCE
1 s at -0.4 V SCE
40 s at -0.2 V SCE

top half: 300 cycle ALD Ir
bottom half: 200 cycle ALD Ir



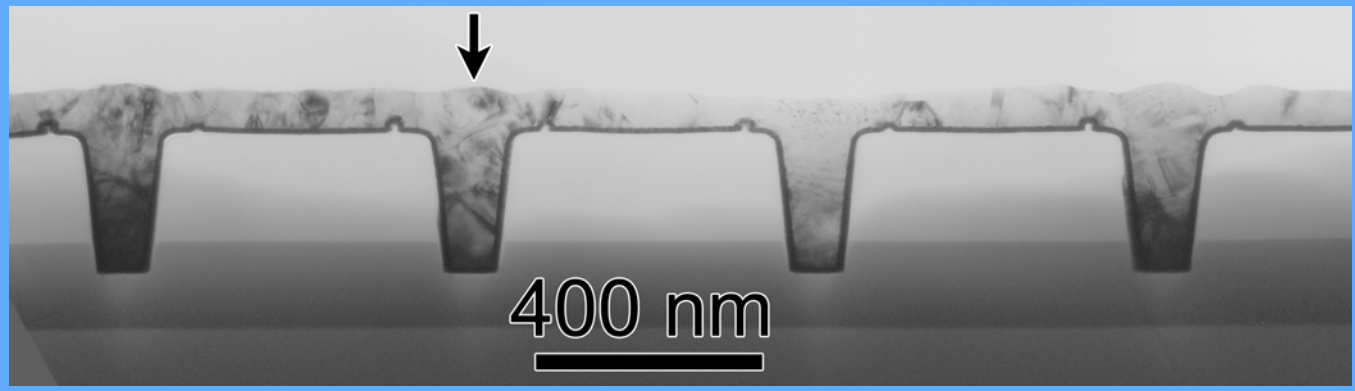
ALD Iridium Barriers



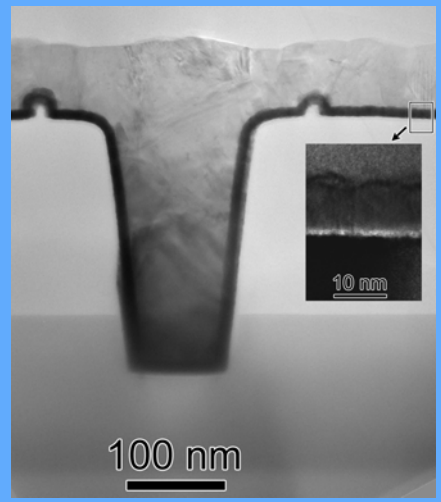
Wetting of Cu deposit on ALD Ir barriers is excellent.

5 s at 0.1 V SCE
1 s at -0.4 V SCE
10 s at -0.2 V SCE

ALD Iridium Barriers



Recrystallization of the Cu conductor is qualitatively similar to that observed on Cu seeded barriers.



Osmium Barriers

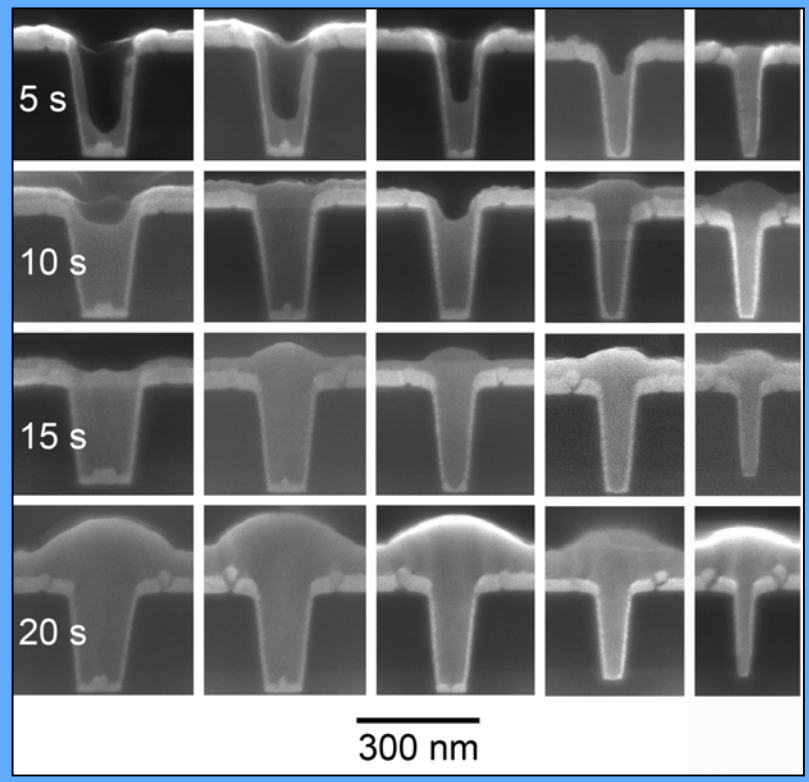
Lane et al. did not mention osmium as a possible barrier for seedless processing. While OsO_4 has its issues, Os has high melting point and thermal and electrical conductivities. It is also immiscible with Cu (<<1 at.% mutual solubilities at 700 °C).

	Melting Temperature K	Electrical resistivity, μΩ cm	Thermal conductivity, W/(m K)
Osmium	3306	8.1	88
Ruthenium	2607	7.1	120
Tantalum	3290	13	57

Other Barriers and Processes

Cu deposition on osmium barriers exhibits a bottom-up superfill geometry that is indistinguishable from that on a Cu seed.

-0.2 V SCE (plating solution) indicated times.

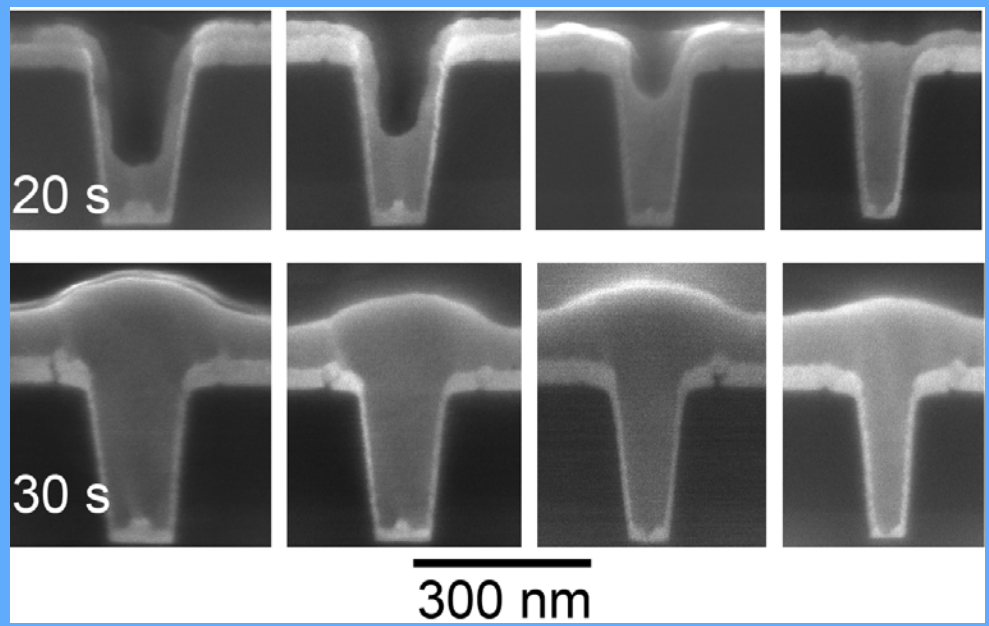


D. Josell, C. Witt and T.P. Moffat, Electrochemical and Solid-State Letters 9, C41 (2006).

Osmium Barriers

One can use different surface pretreatments.

-0.3 V SCE (sulfuric acid) 30 s
-0.2 V SCE (plating solution)
indicated times.

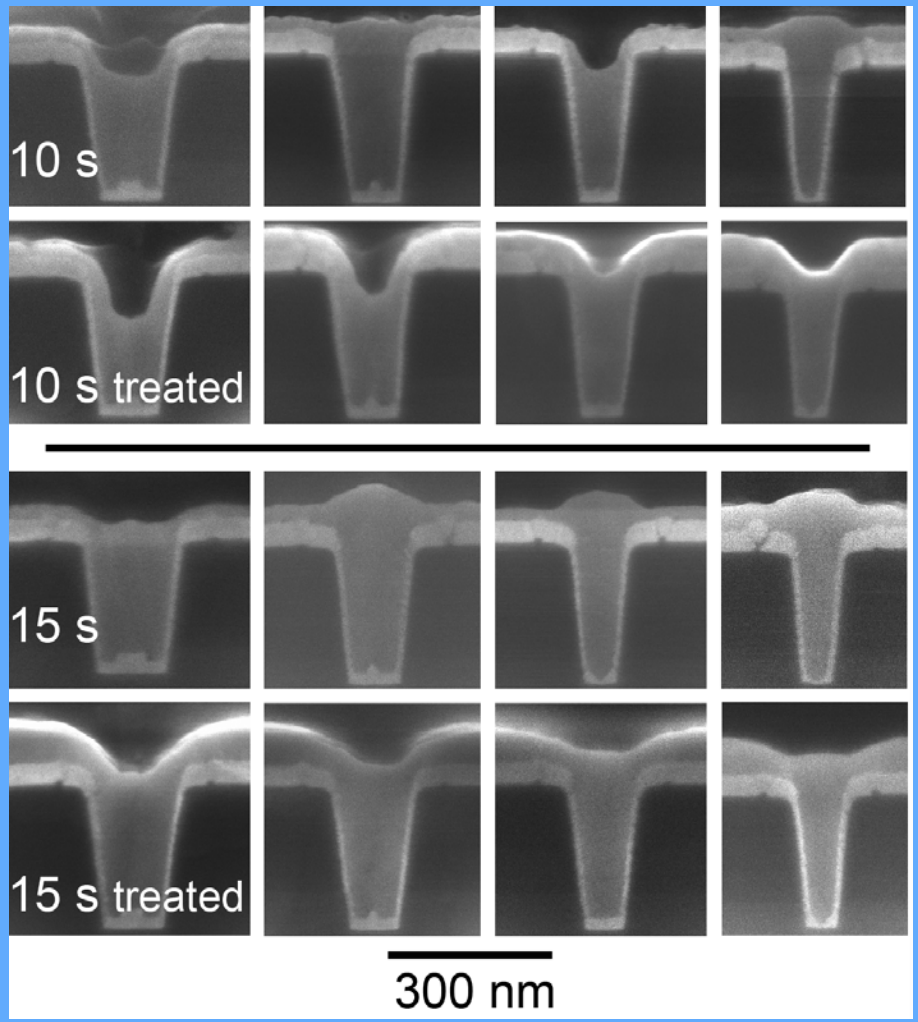


Osmium Barriers

Treatment to remove surface oxide can increase deposition on field, presumably through improved nucleation, with associated decrease in fill within features:

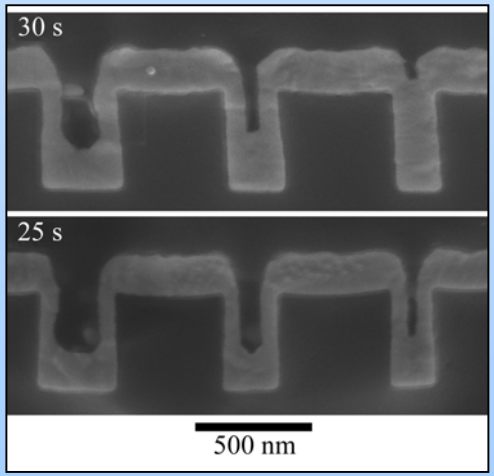
top to bottom:
deposition: -0.2 V SCE 10 s
OPC 30 s before deposition

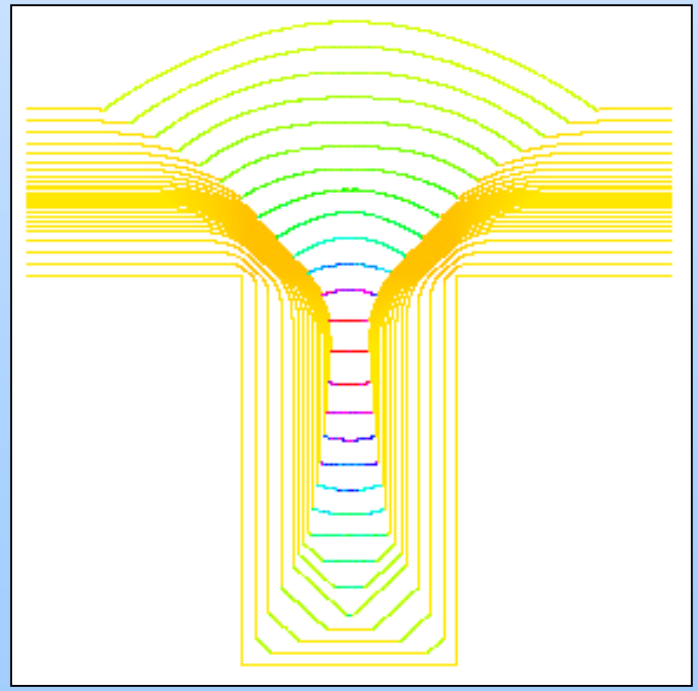
deposition: -0.2 V SCE 15s
-0.3 V SCE sulfuric acid 30s followed by OPC 60 s before deposition.

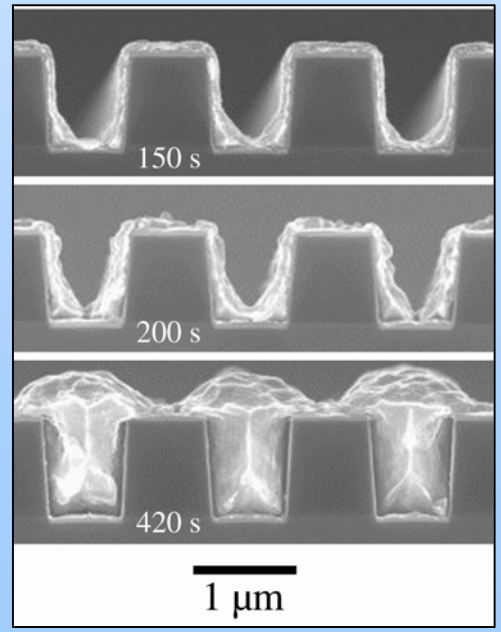


CEAC Modeling of Superfill

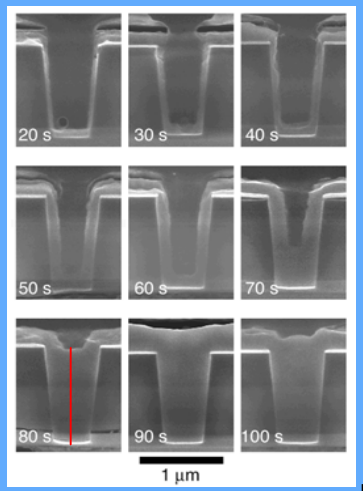
Observed aspects of the superfill phenomenon are the same for these novel barrier materials as for traditional Cu seeded barriers and can be understood using the same CEAC models used to understand Cu superfill on Cu seeds.



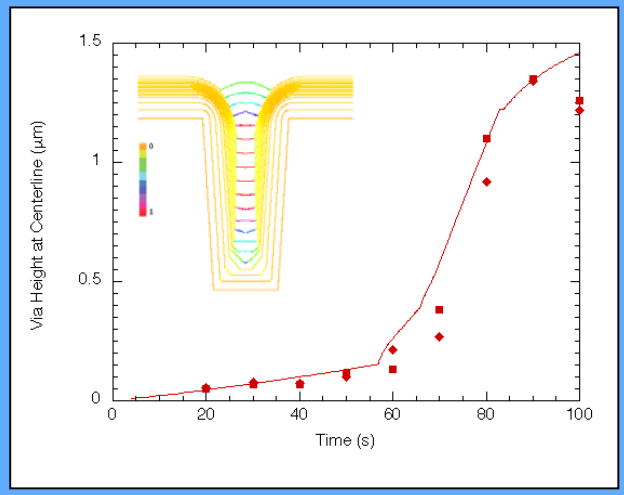




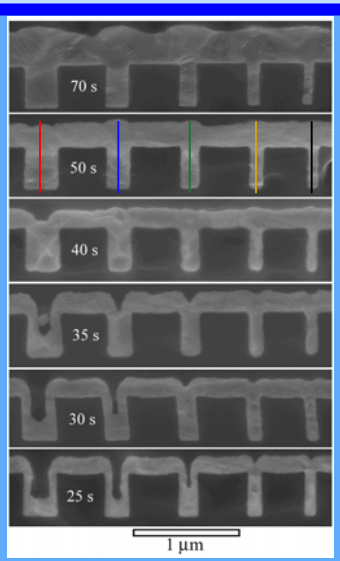
CEAC Superfill



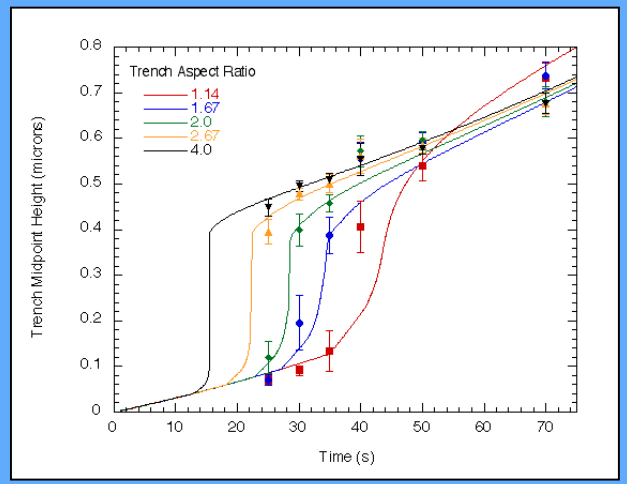
CEAC
Predicts *when* features fill
Time dependence of *via* fill



Copper superfill for Silicon



CEAC
Predicts *which* features fill
Width dependence of *trench* fill



NIST

T.P. Moffat, D. Wheeler, M. Edelstein and D. Josell, IBM Journal of Research and Development 49(1), 19-36 (2005).

Other conductors

The possibility of other conductors for other applications.

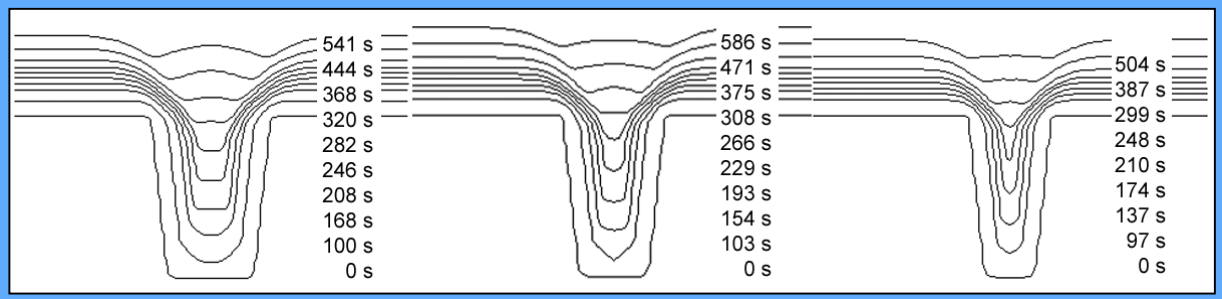
Gold is already used for the ohmic contacts to a variety of wide bandgap semiconductors.

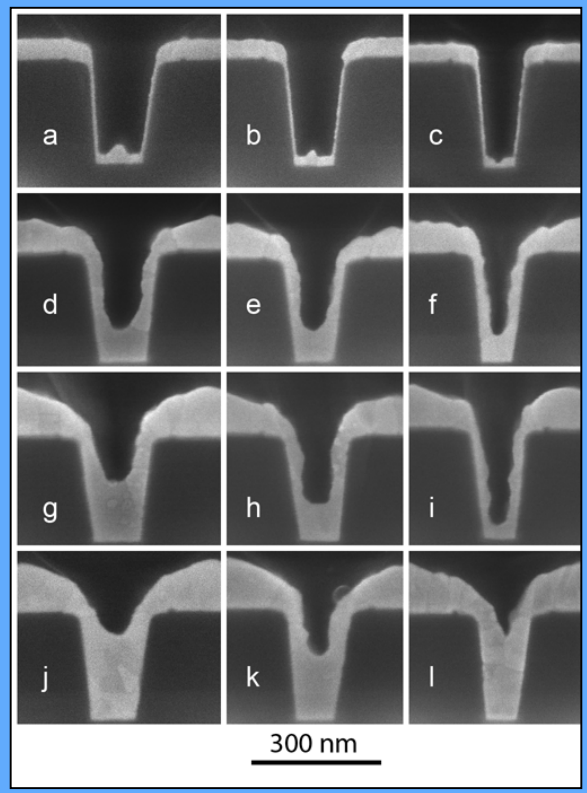
Other Conductors

Gold superfill for GaAs and GaN

Au superfill for damascene processing.

Barrier layer - if good for Cu then...?





D. Josell, C.R. Beauchamp, D.R. Kelley, C.A. Witt and T.P. Moffat, Electrochem. Solid-State Lett. 8(3), C54-C57 (2005).

D. Josell, T.P. Moffat and D. Wheeler, J. Electrochem. Soc. 153, C11 (2006).

Summary

Described motivation and materials for barriers compatible with seedless processing.

What are the properties of these materials as actual diffusion barriers?

- **We have not studied efficacy of these materials as actual diffusion barriers.**
- **Recent reports suggest that 20 nm thick Ru is an effective barrier to temperatures of 450 °C but that more relevant 5 nm thick Ru fails by 300 ° C.**
- **Expect grain boundary diffusion in good quality elemental materials is the problem.**

Summary

Can barrier properties of these materials or similar materials be improved *without substantial negative impact on wettability*?

- **grain boundary stuffing in crystalline layers?**
- **alloying to create amorphous layers?**

Does a material exist that has good wettability, high electrical conductivity, and is an effective diffusion barrier?

- **don't have the faintest idea**
- **any solution will likely involve a tradeoff**

Contributors

NIST (Gaithersburg)	***T.P. Moffat, D. Wheeler, W. Egelhoff, P.J. Chen, M. Perkins (CSTL), C. Richter (CSTL), J.E. Bonevich***
Cookson Electronics - Enthone	***C. Witt***
University of Helsinki, Finland	***T. Aaltonen, M. Ritala, M. Leskela***