Diameter dependent transport properties of gallium nitride nanowire field effect transistors

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The authors report transport property measurements of individual GaN nanowire field effect transistors and the correlation of the electron mobilities with the existence of grain boundaries in these nanowires. Room temperature field effect electron mobilities as high as 319 $cm^2 V^{-1} s^{-1}$ were obtained for the 200 nm diameter nanowires. Mobilities calculated from these reliable nanowire field effect transistors indicated that the surface scattering plays a dominant role in smaller diameter nanowires, whereas for intermediate diameter devices transport is dominated by grain boundary scattering. Reduction of the mobility with decreasing diameter of nanowires can be explained using "continuous surface" model. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2434153]

Nanowires of gallium nitride and other related nitrides with direct band gaps, large breakdown fields, and high saturation velocities are the ideal candidates for efficient nanoscale ultraviolet/visible light emitters, detectors, and radiation hard, high temperature nanoelectronic devices. In the last few years, there has been significant progress in GaN nanowire growth,[1–3] characterization,[4] and individual device fabrication[5–11] though there are very few reports[7,9,10] of detailed transport property measurements in these nanostructures. Correlating the transport properties of these nanowire devices with their structural characteristics is essential for understanding (a) the effects of growth parameters on the device properties and (b) the conduction processes in these nanostructures.

In this letter, we report the results of detailed electrical measurements of GaN nanowire field effect transistor (NWFET) devices, assembled on SiO_2 (600 nm) coated Si substrates utilizing dielectrophoretic forces. The electron backscattered diffraction (EBSD) was used to study the effect of grain boundaries on the transport properties of these nanowires. Diameter dependent electron mobility measurements revealed that larger diameter nanowires exhibited significantly higher mobility than nanowires with smaller diameters. A scattering model, taking into account the surface effects, can explain the observed dependence of mobility on the nanowire diameter.

Nanowires with diameters ranging from 50 to 300 nm and lengths up to 200 μm were grown by direct reaction of metal gallium vapor with flowing ammonia at 850–900 °C in a horizontal furnace.[2] EBSD confirmed that the growth direction of the nanowires was along the *a* axis of the wurtzite structure.[11] A suspension of nanowires in isopropanol, formed by sonication, was dispersed on a 600 nm (thermally grown) SiO_2 coated Si substrate with Ti/Al/Ti (30/100/30 nm) metal pads. Alignment of the nanowires were obtained by applying 20 V peak-to-peak ac voltage at 1 kHz between the metal pads,[12] followed by deposition of a 50 nm SiO_2 passivation layer using plasma enhanced chemical vapor deposition. The oxide was removed over metal-nanowire contact area and a second metal layer (Ti/Al/Ti/Au) (30/100/30/30 nm) was deposited [schematic of NWFET is shown in the inset of Fig. 1(a) and field emission scanning electron microscope (FESEM) image of a complete device is shown in the inset of Fig. 1(b)]. The source drain current (I_{DS}) was measured using a subfemtoampere source measure unit. After the completion of electrical measurements, FESEM was used to study the morphology of the nanowire devices and measure the diameters of the nanowires. EBSD was carried out using the same FESEM at voltages of 15 and 20 keV using an emission current of 20 nA. Software was used to analyze the Kikuchi diffraction patterns and predict the crystal orientation of the nanowires.

Nanowire channel current modulation has been achieved by applying bias to the Si substrate with Al back contacts. Depletion mode behavior with *n*-type conductivity is observed in all devices, possibly due to the presence of lattice defects and impurities such as oxygen. The majority of the NWFETs could not be fully depleted, even at −40 V gate bias, which is often observed with back gated NWFETs,[6–8] due to the poor gate modulation in this geometry. It is possible to completely deplete the channel by using a thinner gate oxide. These devices had high drain-source current (I_{DS}) in the range of 10^{-6}–10^{-5} A for 1 V drain-source voltage (V_{DS}) at 0 V gate-source voltage (V_{GS}) with linear I_D vs V_{DS} characteristics demonstrating Ohmic characteristics of the source drain contacts.[12] Figure 1(a) shows the plot of I_{DS} vs V_{GS} of a nanowire device (diameter of 192 nm, length of 44 μm) with different V_{DS}. Channel current saturation was not observed in these nanowires even at high values of V_{DS}

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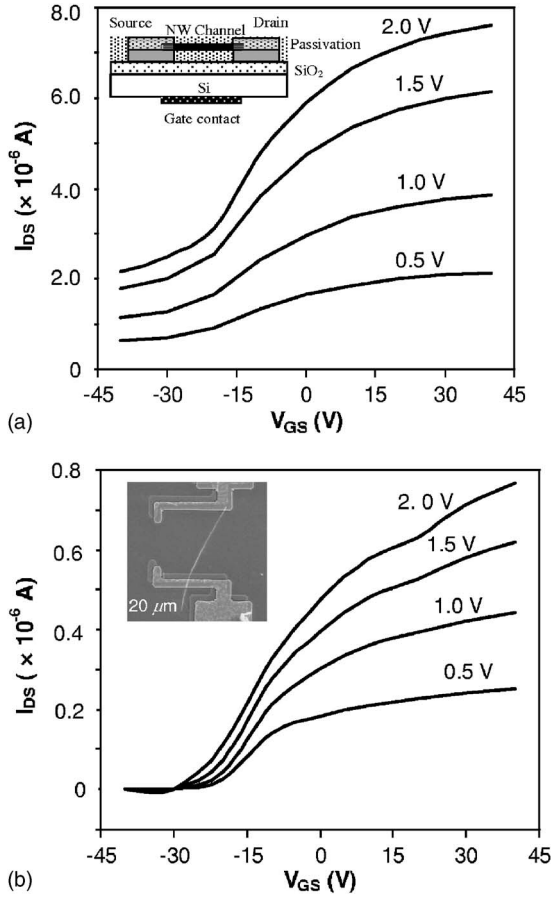

FIG. 1. Transconductance plots (I_{DS} vs V_{GS}) of nanowire FETs with 600 nm gate oxide for different V_{DS} for (a) nanowire with diameter of 195 nm and length of 44 μm with the schematics shown in the inset and (b) nanowire with diameter of 95 nm and length of 35 μm with SEM scan of finished device shown in inset. Value of V_{DS} is shown over each plot.

(±4 V). The electron field effect mobility (μ) is calculated using the relationship[8]

$$\mu = \frac{g_m}{V_{DS}} \frac{L \ln(4t_{ox}/d)}{2\pi\varepsilon_0\varepsilon_{SiO_2}}, \quad (1)$$

where transconductance (g_m) is the slope $\partial I_{DS}/\partial V_{GS}$ of the I_{DS} vs V_{GS} plot measured at $V_{GS}=0$ V and $V_{DS}=1$ V, L and d are the length and diameter of the nanowire, respectively, t_{ox} is the oxide thickness (600 nnm), ε_0 is the permittivity of free space, and ε_{SiO_2} is the permittivity of silicon dioxide. The calculated mobility for this particular device was 230 $cm^2\ V^{-1}\ s^{-1}$. A mobility of 319 $cm^2\ V^{-1}\ s^{-1}$ was calculated for a device with 200 nm diameter nanowire and 56 μm length, which is significantly higher than the majority of the GaN NWFET results published so far,[6–8] except for the report of mobility in excess of 600 $cm^2\ V^{-1}\ s^{-1}$ for GaN nanowire FET by Huang *et al.*[5]

Complete channel depletion at gate voltage of −40 to −30 V with on-off current ratio of 10^7 is only observed in nanowires of diameter of 100 nm and less. Figure 1(b) shows the I_{DS} vs V_{GS} plot of a nanowire device (diameter of 95 nm, length of 35 μm) with V_{DS} varied from 0.5 to 2 V. The electron mobility of this device was 40 $cm^2\ V^{-1}\ s^{-1}$. Mobility measurement on NWFETs with different diameters revealed that mobility in these devices increase with the diameter of the nanowire (Fig. 2). Mobility for 95 nm diameter nanowire was 40 $cm^2\ V^{-1}\ s^{-1}$, whereas mobility of a 200 nm diameter

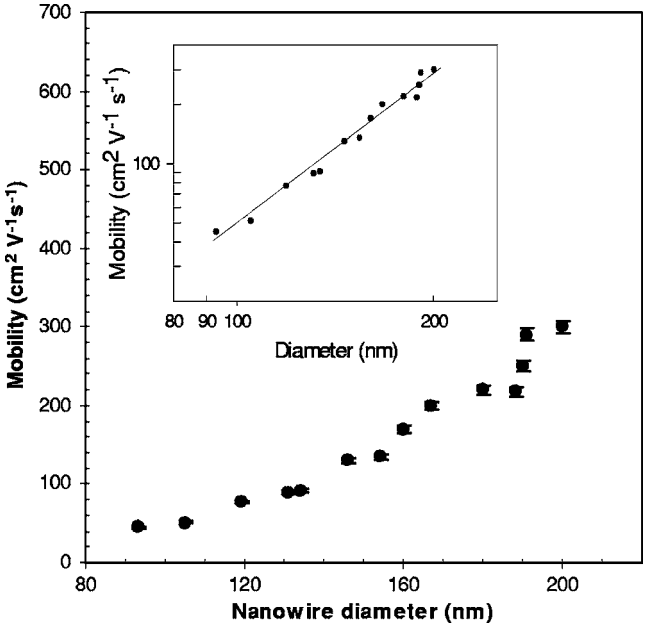

FIG. 2. Plot of GaN nanowire FET room temperature mobility vs nanowire diameter. The inset is logarithmic plot of same curve with slope of 1.3.

nanowire was as high as 319 $cm^2\ V^{-1}\ s^{-1}$. For the devices that could be completely turned off, carrier concentrations calculated using threshold voltage and calculated capacitances[5] were in the range of 2×10^{18} cm^{-3}. Assuming that the background carrier concentration is invariant from one device to another, FET mobility values for 200 nm diameter nanowires are similar to the electron Hall mobility values in GaN epitaxial thin films of equivalent carrier concentrations.[13] Lower mobility in smaller diameter nanowires could be explained by enhanced surface scattering. The effect of sidewall scattering in the overall mobility in these nanowires can be modeled using a simple "continuous surface model."[14] In this model, increased scattering at the surface is accounted for by a surface layer of width w, in which the relaxation time is considerably smaller than that in the interior of the wire. Assuming that surface depletion and surface defects give rise to this surface layer, the width of this layer should remain constant for different wires with the same carrier concentration. The ratio of inner volume to the surface layer volume of a nanowire will be greater in larger diameter nanowires than their smaller diameter counterparts. Hence effective mobilities calculated by averaging the geometric distribution of the relaxation time weighted by the relative carrier concentration will be larger in wider nanowires.

The electron mobility of nanowires as a function of diameter is shown in the inset of Fig. 2 plotted on logarithmic axes. Use of a $\mu \propto d^p$ relationship yields a least squares fit with $p=1.3$. An attempt is underway to understand the physical origin of this relationship. In order to be physically realistic, the plot should asymptotically approach the bulk GaN mobility for larger diameters, with a negative curvature. It is a possibility that additional factors are reducing the mobilities of intermediate diameter nanowires ($120\ \text{nm} \leqslant d \leqslant 160$ nm). In order to investigate such a possibility, after electrical measurements the oxide was completely etched and EBSD was used to study the microstructural properties of all the nanowires devices. It was observed that some of the low mobility nanowires with diameters above 120 nm were

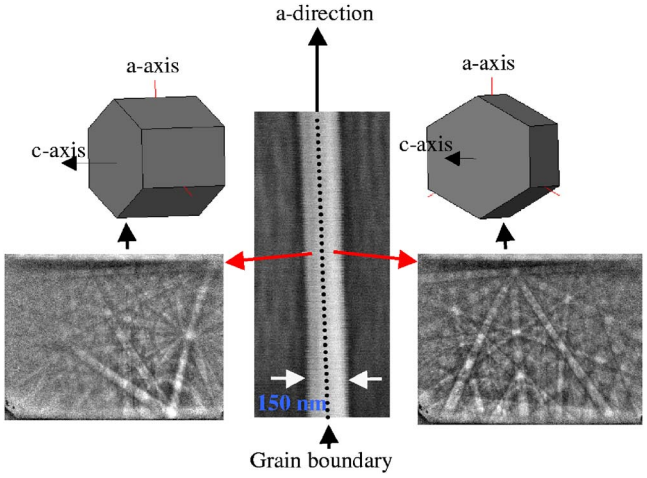

FIG. 3. (Color online) EBSD patterns from two different points on the surface of a 150 nm diameter nanowire. From these patterns, the crystal orientations of the two halves of the bicrystal were determined, as illustrated by the crystal schematics. The *a* axis of each crystal is parallel to the growth direction (as expected) but there is a 42° rotation between the *c* directions about the common *a* axis. The dotted line on the nanowire indicates the grain boundary as inferred from the patterns.

bicrystals with grain boundaries running parallel along the length of the wire. Figure 3 shows the Kikuchi diffraction patterns and the crystal orientations from two different points of a 150 nm diameter nanowire FET device (mobility of 120 $cm^2\ V^{-1}\ s^{-1}$) using EBSD technique. The diffraction patterns did not change when the electron beam was moved along the length of the wire, whereas the diffraction patterns from two different points along the diameter corresponding to the left and right sides of the wire clearly indicated the presence of bicrystals with their *a* axes parallel to the growth direction (as expected) but with a 42° angle of rotation between the *c* directions about the common *a* axis. Higher mobility nanowires studied using EBSD did not reveal the presence of grain boundaries. Grain boundaries were also absent from smaller diameter nanowires.

In summary, transport measurements were performed on individual GaN nanowire transistors having a range of diameters exhibited pronounced size effect in the measured field effect mobility. Room temperature mobility from 40 to 319 $cm^2\ V^{-1}\ s^{-1}$ was measured for nanowires from 95 to 200 nm diameter, respectively. Lower mobility in thinner nanowires (diameter less than 100 nm) can be explained by enhanced surface scattering, whereas EBSD showed that the grain boundary scattering might reduce the mobilities in the intermediate diameter nanowire (diameter between 120 and 180 nm). Further studies are needed to isolate and quantify the effects of surface, grain boundary, defect, and bulk scattering mechanisms on the overall mobility in these nanowire FETs.

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