Nanotechnology **22** (2011) 075206 (10pp) doi:10.1088/0957-4484/22/7/075206

Correlation between the performance and microstructure of Ti/Al/Ti/Au Ohmic contacts to p-type silicon nanowires

Abhishek Motayed[1,2,4], John E Bonevich[1], Sergiy Krylyuk[1], Albert V Davydov[1], Geetha Aluri[3] and Mulpuri V Rao[3]

[1] Materials Science and Engineering Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899, USA
[2] Institute of Electronics and Applied Physics, University of Maryland, College Park, MD 20742, USA
[3] Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030, USA

E-mail: amotayed@nist.gov

Received 2 September 2010, in final form 19 November 2010
Published 14 January 2011
Online at stacks.iop.org/Nano/22/075206

Abstract
Understanding the electrical and microstructural aspects of contact formation at nanoscale is essential for the realization of low-resistance metallization suitable for the next generation of nanowire based devices. In this study, we present detailed electrical and microstructural characteristics of Ti/Al/Ti/Au metal contacts to p-type Si nanowires (SiNWs) annealed at various temperatures. Focused ion beam cross-sectioning techniques and scanning transmission electron microscopy (STEM) were used to determine the microstructure of the source/drain metal contacts of working SiNW field-effect transistors (FETs) annealed for 30 s in the 450–850 °C temperature range in inert atmosphere. Formation of titanium silicides is observed at the metal/semiconductor interface after the 750 °C anneal. Extensive Si out-diffusion from the nanowire after the 750 °C anneal led to Kirkendall void formation. Annealing at 850 °C led to almost complete out-diffusion of Si from the nanowire core. Devices with 550 °C annealed contacts had linear electrical characteristics; whereas the devices annealed at 750 °C had the best characteristics in terms of linearity, symmetric behavior, and yield. Devices annealed at 850 °C had poor yield, which can be directly attributed to the microstructure of the contact region observed in STEM.

S Online supplementary data available from stacks.iop.org/Nano/22/075206/mmedia

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In the last decade silicon nanowire devices have evolved from simple back-gated field-effect transistors [1] (FETs) to the state of the art vertically integrated FETs [2] and novel quantum confined devices [3]. Impressive demonstrations of logic gates [4], electro-optical devices [5], bio-sensors [6, 7], photovoltaic devices [8], and thermoelectrics [9, 10], have been reported using silicon nanowires. The technological potential of these devices and their applications appear almost limitless [11]. In order to realize this potential various aspects of the device structure influencing its performance have to be addressed. One of the crucial components of a nanowire based device is the Ohmic contact. Device performances such as transconductance and high-frequency behavior are often dominated by the parasitic source/drain resistances. Fundamental studies in formation of low-resistance, stable metallization to nanoscale devices are technologically relevant and challenging.

Traditional thin-film silicon metal–oxide–semiconductor field-effect transistors (MOSFETs) have doped source and

[4] Author to whom any correspondence should be addressed.

Table 1. Barrier height and resistivity of Ti, Ni, and their silicides [21–23].

Metal/silicides	Barrier to n-type Si φ_n (eV)	Barrier to p-type Si φ_p (eV)	Resistivity ρ ($\mu\Omega$ cm)
Ti	0.50	0.61	45.0
$TiSi_2$	0.61	0.49	15–20[a]
Ni	0.61	0.51	9.5
NiSi	0.66	0.44	10–15

[a] This resistivity value is for the C54 phase of $TiSi_2$, which has a lower resistivity than the C49 phase.

drain regions which enables the formation of low-resistance Ohmic contacts. Silicon nanowire FETs with *in situ* doped source and drain [12], ion-implanted source and drain [13], and epitaxially grown doped source and drain [14] represent a step in that direction. The other approach is to use metal silicide contacts to SiNW devices. Silicided source/drain contacts are formed by thermally annealing the deposited metals on the ends of the nanowire to form low-resistance silicide phase in contact with the nanowire. Cui *et al* used Ti/Au (50 nm/50 nm) contacts for p-type SiNWs that showed high hole mobilities after annealing the contacts at 300–600 °C in forming gas [15]. Wu *et al* used NiSi contacts to SiNWs to realize FETs with linear characteristics and saturation in the drain current [16]. Weber *et al* demonstrated reduced channel lengths by thermally activated axially intruded NiSi contacts to SiNWs [17]. The formation of platinum silicide at the Pt/SiNW interface has been studied in great detail by Liu *et al* [18]. Lin *et al* demonstrated formation of PtSi/Si/PtSi heterostructures by controlled reaction of SiNWs with lithographically defined Pt pads [19]. All these studies clearly establish the importance of metal silicide based contacts for SiNW devices.

Only three silicides, $TiSi_2$, $CoSi_2$, and NiSi, are currently being considered for the next generation of nanoscale devices. Devices with shrinking dimensions have stringent requirements for contact metallization, such as low resistivity, thermal stability, appropriate Schottky barrier heights for both n- and p-type silicon, and smooth surface morphology suitable for subsequent lithography, which excludes most other silicides [20, 21]. Prior to the deposition of metal films, a 1–2 nm thick native SiO_x layer is usually present on the silicon nanowire surface. The metal in contact with the nanowire is required to first reduce the oxide for the silicide reaction to proceed. Titanium and nickel are capable of reacting with the thin oxide, thus effectively removing the SiO_x layer [20]. Both titanium and nickel silicides have their own advantages and drawbacks, as seen in table 1. There has not been any detailed work on titanium silicide contacts to SiNWs, as compared to nickel silicide based contacts [24].

The focus of this study is to establish a correlation between the electrical performances of Ti based contacts to p-type SiNW devices with their microstructural characteristics resulting from annealing. In this paper, we present detailed electrical characterization of p-type SiNW back-gated FETs with source/drain contacts formed by depositing Ti/Al/Ti/Au (70 nm/70 nm/30 nm/30 nm) and annealing them at temperatures ranging from 450 to 850 °C. In this four-layer design, the first Ti layer in contact with the semiconductor is for the silicidation, the Al layer is placed to reduce the contact resistance of the total metallization stack, and the top two Ti and Au layers are used to protect the Ti/Al layers from oxidation and to facilitate reliable device probing. Scanning transmission electron microscope (STEM) images of the focused ion beam (FIB) cross-sectioned metal/SiNW contact regions of working devices were collected. Chemical analysis and diffraction techniques were used to characterize these cross-sections. As-deposited contacts, and contacts annealed at 550, 750, and 850 °C were studied to identify the extent of metal interdiffusion and reaction with SiNW, and to image the evolution of the metal/NW interface with the change in annealing temperature.

2. Experimental details

The SiNWs were grown in a hot-walled chemical vapor deposition system. Commercially available 100 nm Au nanoparticles were cast on poly-L-lysine-functionalized p-Si(111) substrates with native oxide. Nanowire growth was performed at 850 °C and pressure 80 kPa (600 Torr) using 30 sccm (standard $cm^3\ min^{-1}$) of silicon tetrachloride and 200 sccm of hydrogen diluted with nitrogen to a total flow rate of 1000 sccm. Silicon tetrachloride vapor was delivered by bubbling nitrogen through a bubbler held at 10 °C and 104 kPa (780 Torr). The p-type doping of SiNWs was accomplished by passing 200 sccm of hydrogen over a sapphire boat with B_2O_3 powder held at 840 °C. Despite the fact that these temperatures are too low to obtain a sufficient B_2O_3 flow (B_2O_3 vapor pressure is $\sim 10^{-4}$ Pa (10^{-6} Torr) at 850 °C) [25], the hydrogen induced transformation of boron oxide into boric acid, whose vapor pressure is much higher, allows for efficient p-doping to be achieved [26].

Post-growth device fabrication was done by dielectrophoretically assembling the nanowires on a heavily doped p-type Si substrate which had 1.2 μm thick thermally grown SiO_2 on top of it [27]. This substrate had 10 nm thick Ti alignment electrodes with gaps ranging from 5 to 25 μm. A suspension of the nanowires in isopropanol (IPA) was formed by sonicating the growth substrate in IPA for 10 s. The suspension was dropped onto the device substrate with two 10 V peak-to-peak sinusoidal signals with 1 kHz frequency and 180° phase difference applied across the pads. After the alignment step, the samples were dried at 75 °C for 10 min on a hot plate to ensure the complete evaporation of the residual solvent. The samples were then cleaned in Ar plasma with 25% O_2 for 10 min. This was followed by a sputter deposition of 50 nm of SiO_2 which encapsulated all the devices. The deposition was done at room temperature and at a pressure of 0.2 Pa (2×10^{-3} Torr). This oxide layer passivates the devices yielding reproducible device measurements. After the oxide deposition, a photolithography step was performed to define the opening for the top contact. The oxide on the opening was etched using reactive ion etching (RIE) with $CF_4/CHF_3/O_2$ (50 sccm/25 sccm/5 sccm) gas chemistry. The top contact metallization stack was deposited in an electron beam evaporator with a base pressure of 10^{-5} Pa (1×10^{-7} Torr). The deposition sequence was Ti (70 nm)/Al

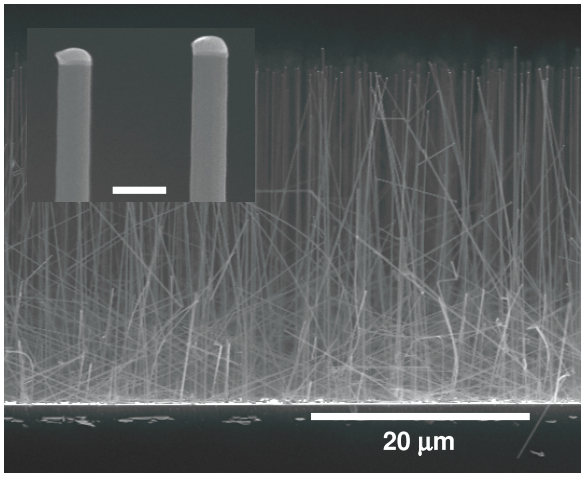

Figure 1. FE-SEM image of SiNWs grown on a silicon substrate. The wires are on average 30 μm long. The inset is the high magnification image of NWs with Au-caps (the scale bar is 200 nm).

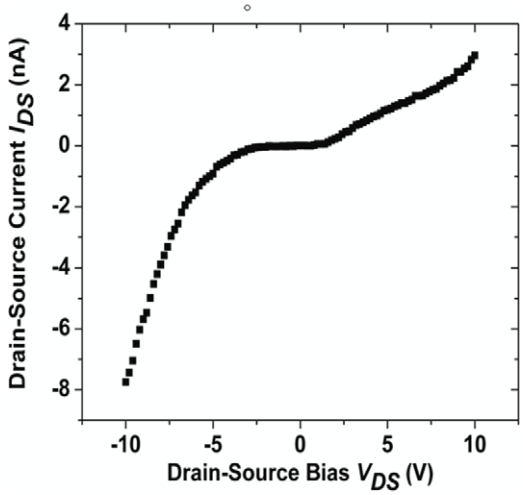

Figure 2. Typical electrical characteristics of SiNW FETs with as-deposited contacts. I_{DS} versus V_{DS} characteristics of a single SiNW FET with diameter 150 nm and length 6 μm. For the measurement the source and gate were connected together and held at 0 V.

(70 nm)/Ti (30 nm)/Au (30 nm). Thermal annealing of the complete devices was done in a rapid thermal processing system with 6 slpm (standard liter per min) flow of ultrahigh purity Ar. The annealing temperature was varied from 450 to 850 °C with a constant hold time of 30 s and constant ramp rate of 100 °C min^{-1}. This relatively slow ramp rate was chosen to reduce stress in the metal–nanowire contact area during heating. The device characterization was done using an Agilent B1500A semiconductor parameter analyzer connected to a probe-station[5]. After completing the electrical measurements, the top SiO_2 layer was removed by a RIE etching step using the same chemistry as described earlier. The nanowire dimensions were measured by FE-SEM in order to estimate the mobility and the carrier concentration in the nanowires.

In order to gain an insight into the processes responsible for the changes in the contact properties due to annealing, we employed scanning transmission electron microscopy (STEM) techniques to study the contacts of the devices annealed at 550, 750, and 850 °C. For comparison purposes we also looked at as-deposited contacts. Cross-sectional samples suitable for characterization by STEM were prepared by site specific *in situ* lift-out methods in a focused ion beam instrument (FIB) [28], and subsequently observed in a 300 kV TEM/STEM instrument. The TEM/STEM was equipped with an x-ray energy dispersive spectrometer (XEDS) as well as a high angle annular dark-field (HAADF) detector to perform mapping of variations in composition and microstructure, respectively. The phase analysis of the annealed metallization layers was done using x-ray diffraction (XRD). The XRD scans were collected on a Bruker-AXS D8 scanning x-ray micro-diffractometer equipped with a general area detector diffraction system (GADDS) using Cu Kα radiation (see footnote 5). The two-dimensional 2Θ–χ patterns were collected in the 2Θ = 25°–56° range followed by integration into conventional Ω–2Θ scans.

[5] Certain commercial equipment instruments or materials are identified in this paper to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

3. Results and discussions

Figure 1 shows a cross-sectional field-emission scanning electron microscope (FE-SEM) image of SiNWs grown for 30 min with a growth rate of 1.2 μm min^{-1}. The average diameter of SiNWs was ca. 135 nm and the difference between base and tip diameters was ca. 5 nm, implying a very slow rate of uncatalyzed silicon deposition on the sidewalls [29].

The I–V characteristics of all the as-deposited devices showed similar characteristics. The I–V curves were nonlinear, asymmetric, with a barrier which can be clearly seen at low biases (figure 2). This is not surprising considering the fact that the barrier height of Ti to p-type Si is 0.61 eV (see table 1). The presence of a thin native interfacial oxide would require tunneling of the carriers through it, which would contribute to the barrier to the current flow. The transconductance plots (I_{DS} versus V_{GS}) only showed weak p-type behavior for all the devices (not shown here). This might be due to the fact that the contacts were highly resistive, thus the channel current modulation by the gate is masked by the high parasitic contact resistances.

After annealing the samples at 450 °C for 30 s, small improvements in the I–V characteristics were seen in the devices. The barrier at low bias was reduced but did not disappear completely (see figure 3). Although we might not expect significant metal–nanowire reaction at 450 °C, it has been shown that the Ti starts to reduce a thin interfacial SiO_X layer on Si, and form stable interfacial silicides even at temperatures as low as 300 °C [30]. Solid titanium is known to dissolve up to 33 at.% of oxygen in a solid solution at elevated temperatures [31]. This ability of Ti to readily reduce native interfacial oxide is beneficial for the contact formation. Most of the devices showed gate voltage induced modulation of the channel current with polarity consistent with p-type majority carrier.

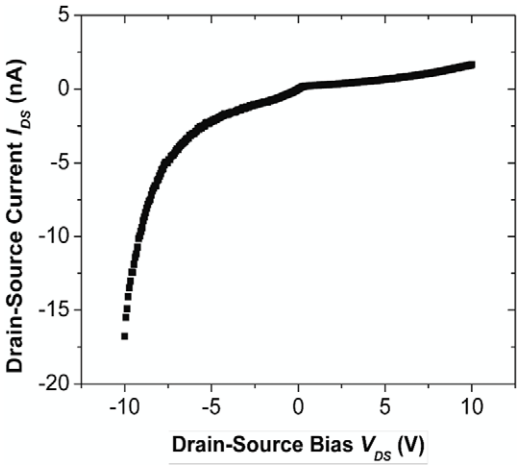

Figure 3. Typical electrical characteristics of SiNW FETs with contacts annealed at 450 °C (NW diameter 120 nm and length 8 μm).

The devices annealed at 550 °C for 30 s showed significant changes in their I–V characteristics, with the majority of the devices exhibiting linear I–V curves. For all the devices, the gate bias modulation of the channel current was significant. The channel current decreased with increasing positive gate bias for all the devices, as expected for the p-doped SiNWs. It is worth mentioning that the ambipolar behavior is not observed in these nanowire FETs even for gate biases higher than 15 V. Ambipolar transport is often observed in metal-contacted Schottky barrier MOSFETs [14, 19, 32, 33], where the channel current is not determined by the channel potential, but rather dominated by carrier injection, by thermal emission of carriers over the barrier and thermally assisted tunneling through the barrier [11]. This is also the reason that in Schottky barrier FETs the channel current saturation at high channel biases is usually not observed. Figure 4 shows the typical device characteristics from SiNW FET with contacts annealed at 550 °C for 30 s. Although the current decreased significantly with positive gate bias, a complete depletion effect is not observed in these devices at +15 V V_{GS}. As evident from the figure, the channel current for this device saturated around +2.5 V and −5 V V_{DS}. This type of saturation behavior is observed in approximately 40% of the total number of working devices. The fact that we observe the drain current saturation behavior in these devices indicates that the channel current is not dominated by the Schottky barrier at the source and drain contact.

Field-effect hole mobility (μ) is calculated using the relationship $\mu = g_m L^2/C_g V_{DS}$, where g_m is the transconductance obtained from the slope of I_{DS} versus V_{GS} plot, L is the device length, C_g is the gate capacitance, and V_{DS} is the drain–source voltage at which the g_m is measured. The gate capacitance for the back-gated NW FET embedded in a dielectric can be estimated using the analytical expression $C_g = (2\pi\varepsilon_0\varepsilon_r)/\cosh^{-1}(1+t_{ox}/r)$, where ε_0 is the permittivity of free space, ε_r is the dielectric constant of the embedding dielectric, t_{ox} is the thickness of the back-gate oxide, and r is the radius of the nanowire [34]. The mobilities calculated for

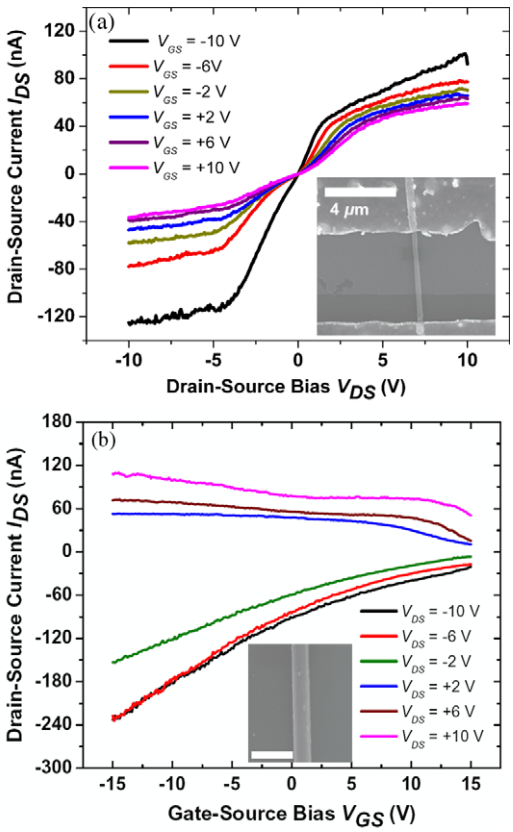

Figure 4. (a) I_{DS} versus V_{DS} characteristics as a function of gate voltage V_{GS} of a SiNW FET with contacts annealed at 550 °C. (b) I_{DS} versus V_{GS} characteristics as a function of drain–source bias V_{DS}. Insets in (a) and (b) show, respectively, low- and high magnification FE-SEM images of the SiNW device with diameter 220 nm and length 6 μm. The scale bar in the lower inset is 500 nm.

all the nanowires were in the range of (0.3–0.5) cm^2 V^{-1} s^{-1}. The carrier concentration (p) can be calculated by considering the relationship $p = V_{th}C_g/qAL$, where V_{th} is the threshold voltage for the device. For accumulation mode MOSFETs, V_{th} is the gate voltage for which the channel current is reduced to zero. Only a few of the devices showed complete depletion of the channel current with high positive gate voltage, and the hole concentrations calculated for those devices were in the range of (2.0–3.0) × 10^{17} cm^{-3}. The hole mobility for the present devices is significantly lower than the values reported for p-type SiNW FETs [14, 19, 32, 33]. There are few reports of low hole mobility values in boron-doped SiNWs that are in the same range as ours [27, 35]. Transmission electron microscopy has confirmed that these nanowires are single crystals with a very low density of structural defects (see supporting information available at stacks.iop.org/Nano/22/075206/mmedia). Surface scattering might be present but cannot be the dominant factor for such large diameter nanowires [36]. One of the possible causes of high resistivity and low mobility in these SiNWs could be the formation of deep levels due to possible diffusion of catalytic gold into the silicon matrix. The two main levels produced by Au in silicon are an acceptor level at 0.54 eV below the conduction band and a donor level at 0.35 eV above the valence band [37]. Although

Table 2. Summary of the characteristics of samples annealed at different temperatures.

Annealing temperature (°C)	Linear (%)[a]	Symmetric (%)[b]	Yield (%)[c]	Total number of devices measured
As-deposited	—	—	—	45
450	—	—	10	20
550	50	15	30	40
650	60	15	45	35
750	77	22	75	45
850	—	—	<1	40

[a] Ratio of devices with linear I–V characteristics for ±1 V V_{DS} to the total number of conducting devices expressed in per cent.
[b] Ratio of devices with I_{DS} at 10 V V_{DS} which is ±20% of I_{DS} at −10 V V_{DS} to the total number of conducting devices expressed in per cent.
[c] Ratio of conducting devices to the total number of NW devices expressed in per cent. For as-deposited and 450 °C annealed samples '—' indicates that there were no devices with that property. We have not calculated yield for the as-deposited sample. Devices annealed at 850 °C showed poor yield (less than 1%) and were neither linear nor symmetric. The total number of devices measured for each annealed temperature is also given.

it has not been experimentally verified [36], Au could diffuse into the SiNW during the growth. From the thermal diffusion data in the Au–Si system [38] we have estimated that at 850 °C the equilibrium solid solubility of Au in Si is 2×10^{15} cm^{-3} (4×10^{-6} at.% Au). Majority of the gold atoms will be electrically active according to the 'kick-out' model, which indicates that virtually all the Au is present in the substitutional form in the Si matrix [38]. This will result in partial compensation of the boron atoms, thus increasing the resistivity of the nanowires. The hole mobility at room temperature will also be reduced due to the ionized impurity scattering by the Au donor atoms [39]. Temperature dependent transport, generation–recombination noise, and photoconductivity measurements are currently being pursued to identify the cause of such low mobility in these devices.

Figure 4(b) reveals an important characteristic of the devices annealed at 550 °C. The majority of the devices showed asymmetric behavior. For future large-scale integration of nanowire based devices, symmetric device characteristics are essential. To promote the formation of silicide and/or intermetallic reactions, which could be responsible for the improvements of the contact properties, we continued annealing the devices at higher temperatures. Table 2 summarizes the important characteristics for a large number of devices annealed at temperatures from 450 to 850 °C. As evident from table 2, the contact properties showed a steady improvement with annealing temperature. For devices annealed at 750 °C, a majority of the devices had linear characteristics and a large number of devices had symmetric behavior.

Figure 5 shows the characteristics from a typical device annealed at 750 °C. The symmetric nature of the contact properties is clearly seen. Hole mobility and concentration for devices annealed at different temperatures were in the same range. Transconductance normalized to the gate width for this device for 10 V V_{DS} is 300 μS μm^{-1}, which is

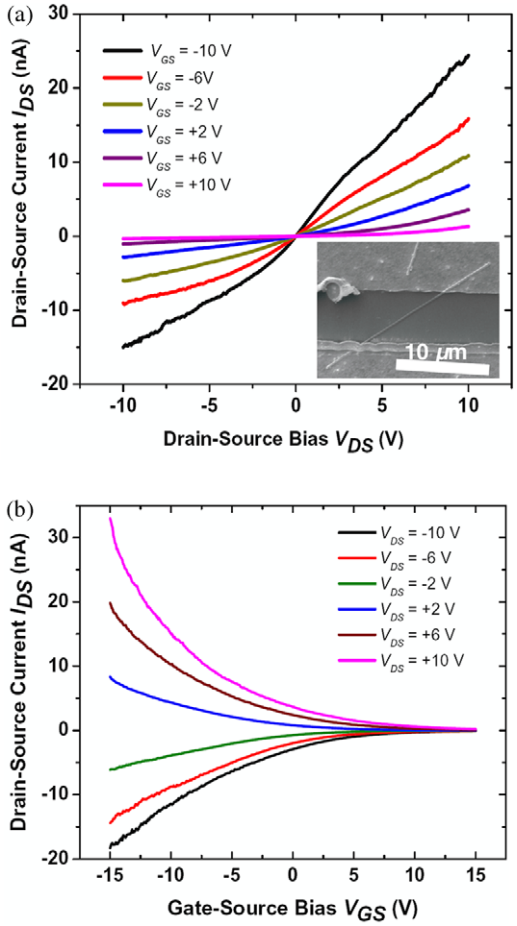

Figure 5. (a) I_{DS} versus V_{DS} characteristics as a function of gate voltage V_{GS} of a SiNW FET (diameter 100 nm and length 10 μm) with contacts annealed at 750 °C for 30 s. The inset is the FE-SEM image of the device. (b) I_{DS} versus V_{GS} characteristics as a function of drain–source bias V_{DS}.

comparable to the other reported results using p-type Si nanowire channel [2, 32].

The as-deposited nanowire contact shown in figure 6 clearly reveals the layers of the Ti/Al/Ti/Au metallization. The HAADF signal is highly sensitive to local variation in average atomic number (proportional to Z^2) as well as microstructural variation such as grain size (channeling contrast). While the metallizations show discrete layering far away from the nanowire, the layers surrounding the nanowire reveal density variations and pinhole gaps. The XEDS maps (see figure 7) agree well with the expected metallization layers. However, XEDS profiles do suggest a small amount of reaction between the Ti layer adjacent to the top of the Si nanowire.

In contrast, the nanowire contacts annealed at 550 °C revealed significant interdiffusion of the metals and the onset of their reactions with the nanowire (see figures 8 and 9). Standardless analysis of the XEDS signal unambiguously confirmed intermixing of Si with Ti and to a smaller degree, with Al and Au at the metal/nanowire interface. The identification of interfacial reaction products was not possible due to the complex nature of the diffraction patterns in

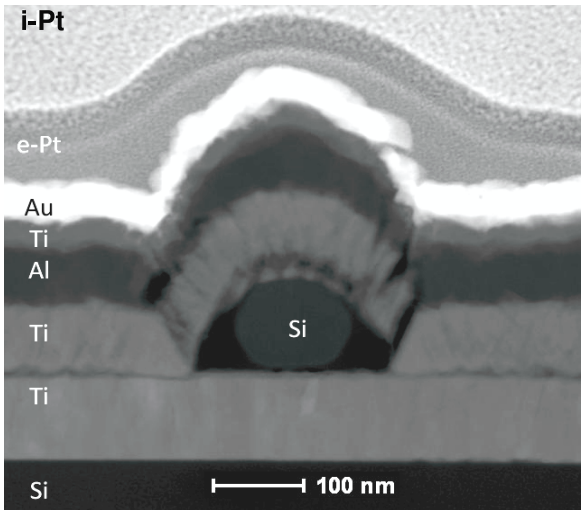

Figure 6. HAADF-STEM image of as-deposited nanowire contacts. For this particular sample the bottom Ti layer that resides on the silicon substrate was 100 nm thick. This was done to compare the morphology of Ti layers deposited on a silicon flat substrate versus on SiNW. For all the annealed samples the bottom Ti layer was 10 nm thick. Note that the two top Pt layers are deposited as part of the standard FIB cross-sectioning procedure (the electron beam assisted and the Ga ion beam induced Pt layers are labeled e-Pt and i-Pt, respectively).

STEM. Given the complex nature of the interdiffusion between the metal layers and compositional gradients formed during annealing, we have limited structural and chemical analyses in STEM to identify the transformations occurring near the original Ti/Si interface.

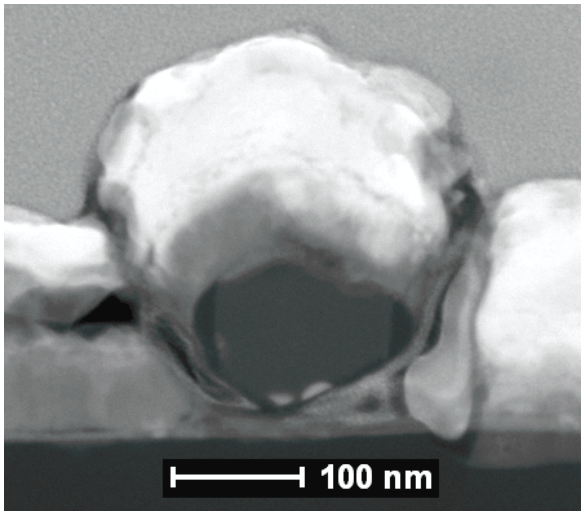

Figure 8. HAADF-STEM image of Si nanowire contacts annealed at 550 °C. Interdiffusion between the metal layers and their reaction with Si has started.

According to x-ray diffraction (XRD) analysis (see figure 10), two intermetallic compounds were formed as a result of metal interdiffusion: AlAuTi (hexagonal phase, $B8_2Ni_2In$-type, with $a = 0.4407$ nm and $c = 0.5829$ nm) and Al_3Ti (metastable cubic phase, $L1_2Cu_3Au$-type, with $a = 0.4103$ nm). Possible silicide formation resulting from metal reaction with the nanowire (as observed in STEM in figure 9) was not detected in XRD, which is expected considering the miniscule amount of silicides formed. Annealing at higher

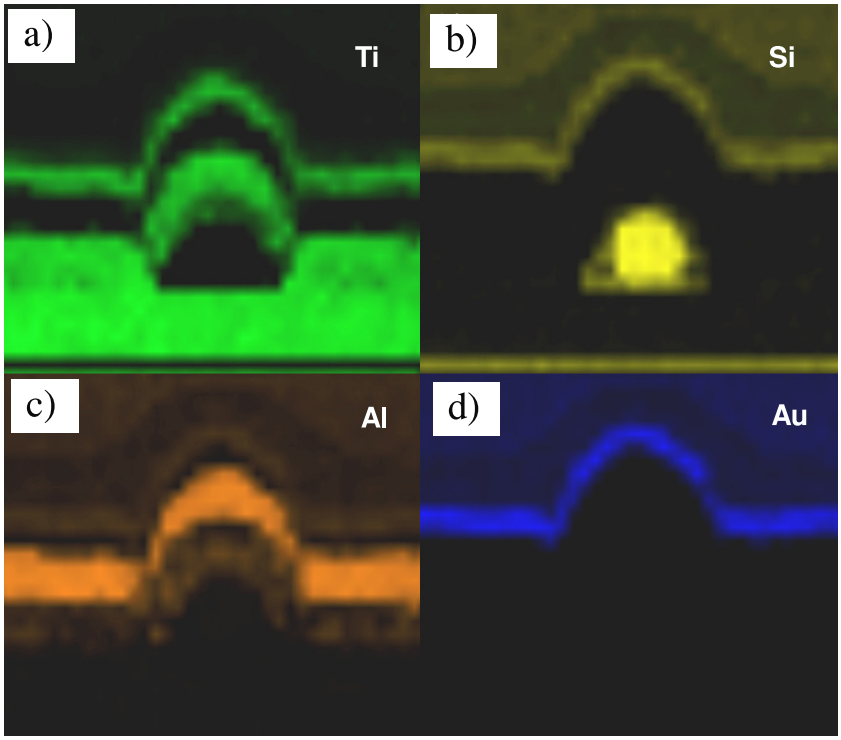

Figure 7. Corresponding XEDS elemental maps: (a) Ti, (b) Si, (c) Al, and (d) Au. In image (b) the Si signal shows up in the Au layer. This is an artifact resulting from the peak overlap of the Si–K and Au–M lines.

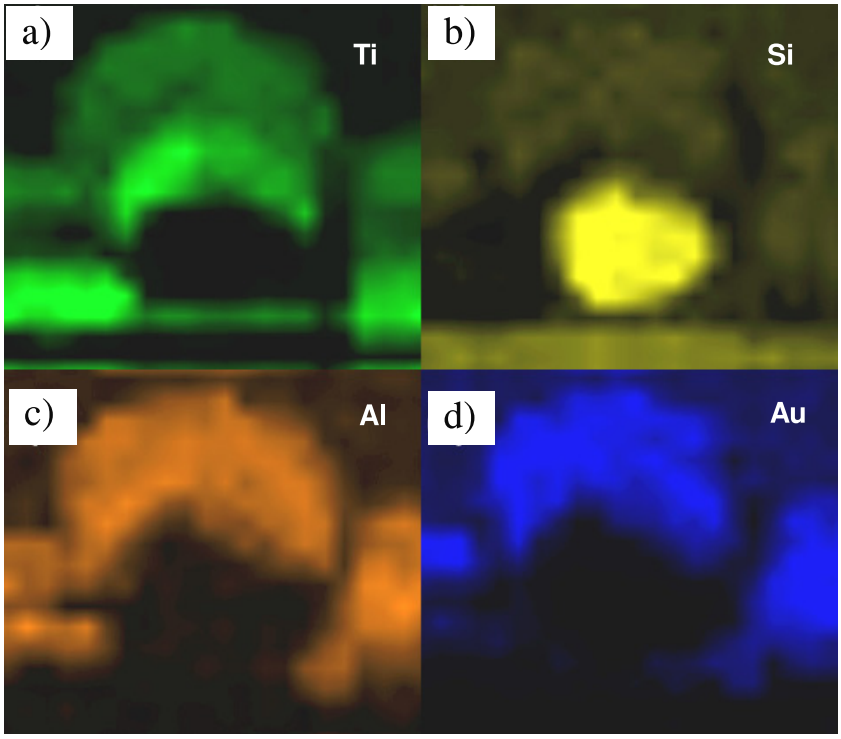

Figure 9. Corresponding XEDS elemental maps: (a) Ti, (b) Si, (c) Al, and (d) Au. The artifact resulting from the peak overlap of the Si–K and Au–M lines is visible in image (b).

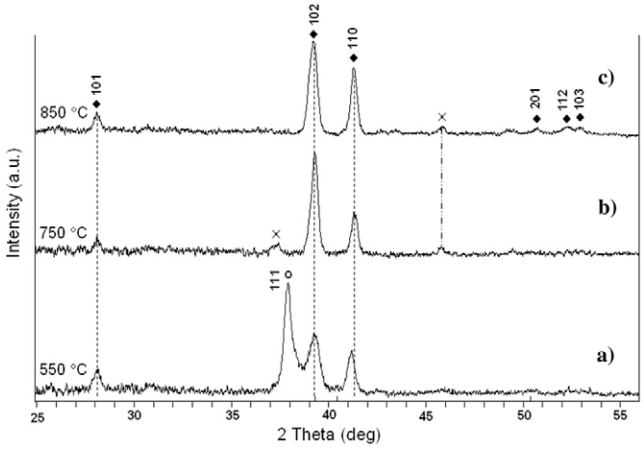

Figure 10. XRD spectra of Ti/Al/Ti/Au contacts annealed at (a) 550 °C, (b) 750 °C and (c) 850 °C. The 550 °C sample consists of AlAuTi (♦) and Al_3Ti (o) phases; the 750 and 850 °C samples consist of AlAuTi (♦) and traces of unidentified phases (×). Note since XRD spectra for samples annealed at 450 and 650 °C look very similar to the 550 °C sample spectrum, they are omitted for clarity.

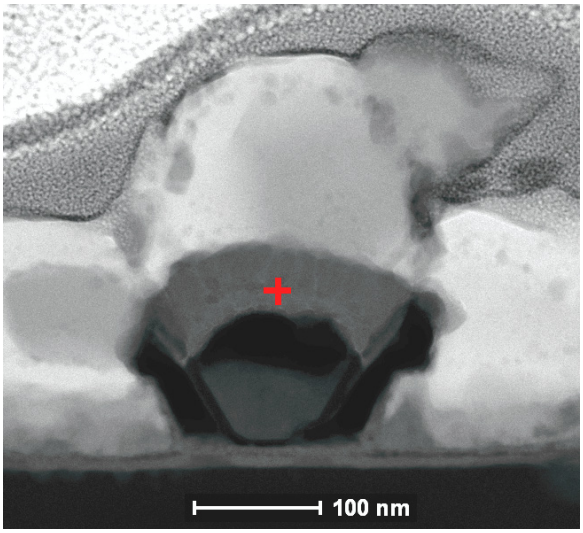

Figure 11. HAADF-STEM image of Si nanowire contacts annealed at 750 °C. The nanowire is almost 50% consumed by the Ti overlayer. The bottom facets of the nanowire are still clearly visible. Metals have completely interdiffused. XEDS and diffraction analyses for figure 12 were performed at the red cross mark.

temperatures induced further transformations in the metal layers. Compared to 450, 550 and 650 °C (see figure 10), annealing at 750 and 850 °C leads to formation of AlAuTi and to the disappearance of the Al_3Ti phase. The fact that both 750 and 850 °C anneals resulted in completion of metal reactions, converting a 4-metal stack to almost a single AlAuTi phase, makes the selected Ti/Al/Au/Ti contact thermally stable in the 750–850 °C temperature range.

Microstructural analysis of the 750 °C annealed metal/nanowire interface revealed that almost 50% of the metal-coated portion of nanowire was consumed (see figure 11). The dark region above the residual nanowire represents a void, which likely resulted from silicon out-diffusion into the titanium layer, as evident from the XEDS maps in figure 12. The void formation can be explained by the fact that Si, as

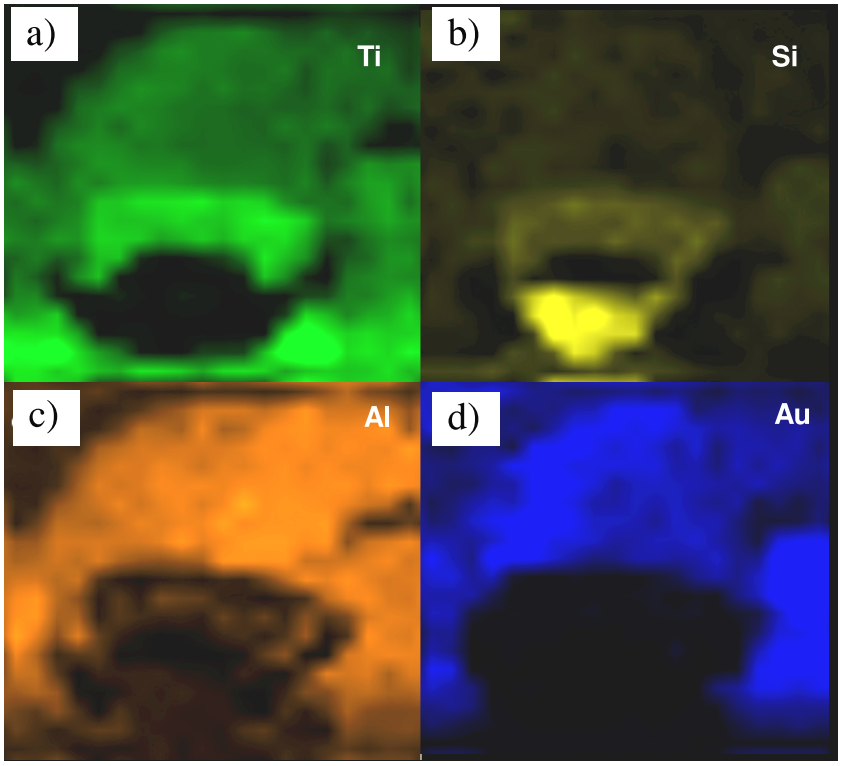

Figure 12. Corresponding XEDS elemental maps: (a) Ti, (b) Si, (c) Al, and (d) Au.

the dominant diffusion species in the Si–Ti system [40, 41], migrates into the Ti-rich layer, leaving a 'Kirkendall void' in the nanowire. While a similar void formation was observed in planar Si/Ti thin-film structures [42–44], this is the first reported observation of the Kirkendall-effect-induced hollowing in a silicon nanowire.

Standardless analysis of the XEDS signals reveals that the area near the red marker in figure 11, which is representative of the 50 nm thick dark-gray layer above the nanowire void, contains approximately 57 at.% Ti, 41 at.% Si, and traces of Al and Au. Microstructural analysis indicates that this layer consists of a multiphase mixture with polycrystalline and amorphous components. Due to this complexity, unambiguous phase identification was not possible. The complexity of this Ti–Si based reaction layer was anticipated and could be easily related to the wealth of experiments in planar Ti/Si bi-layer annealing experiments. The interface in Ti/Si thin-film diffusion couples often has grading composition between 30 and 70 at.% Ti, and consists of intermetallic Ti_5Si_3, Ti_5Si_4, TiSi, $TiSi_2$, and amorphous phases [45–49]. The fact that our Ti and Si composition values are close to the Ti_5Si_3 and Ti_5Si_4 stoichiometries also agrees with the above references that these two compounds often form first among the transient phases when the Ti/Si bi-layer is subjected to heat treatment.

The most significant transformation of the nanowire morphology was revealed in the STEM image of the nanowire contact annealed at 850 °C (see figures 13 and 14). Almost complete out-diffusion of the Si from the nanowire is observed. This is not surprising considering the morphology of the nanowire-contact cross-section observed for the 750 °C annealed sample. The nearly complete hollowing-out of the nanowire under the metal contacts due to the Kirkendall effect is most likely the primary cause of the failure of the devices annealed at 850 °C.

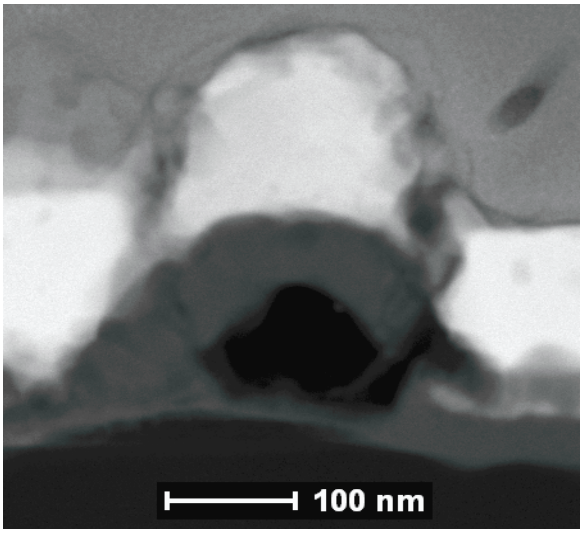

Figure 13. HAADF-STEM image of Si nanowire contacts annealed at 850 °C. The nanowire is almost completely consumed by the reaction with metal layers.

In light of the STEM analysis, we assume that the significant improvement of the electrical characteristics for the devices annealed at 750 °C as compared to lower temperature anneals, was possibly associated with formation of silicides in the SiNW adjacent layer: the intermixing of Si with Ti,

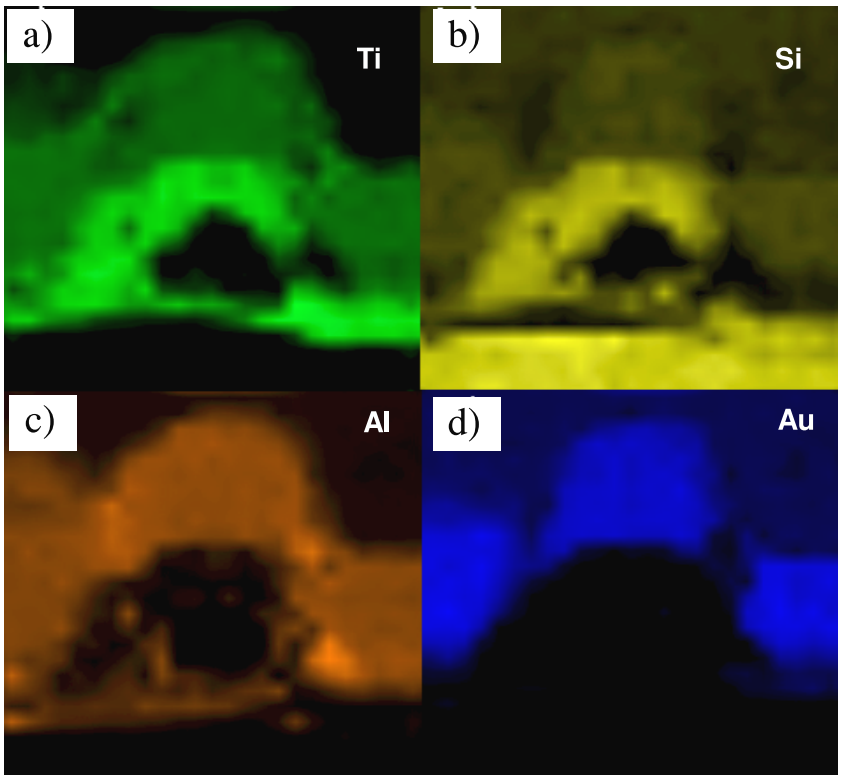

Figure 14. Corresponding XEDS elemental maps: (a) Ti, (b) Si, (c) Al, and (d) Au.

and to a smaller degree with Al and Au. These effects were much more pronounced for the 750 °C annealed sample (see figures 11 and 12) as compared to the 550 °C anneal (figures 8 and 9). Also, the potentially detrimental effect of Kirkendall-induced voids in the nanowire on its electrical properties was revealed in this study. The interplay between the beneficial silicide formation and the detrimental nanowire voiding at elevated temperatures was manifested at the highest annealing temperature of 850 °C. The low electrical yield obtained for the 850 °C annealed devices could be clearly associated with the severe void formation ultimately leading to the failure of the contacts. To the best of our knowledge, this is the first direct observation of the contact failure mechanism due to Kirkendall voiding in nanowire devices.

4. Conclusions

In conclusion, we have studied the microstructural evolution of Ti/Al/Ti/Au contacts to SiNW FETs in the 450–850 °C temperature range using XRD and STEM, and correlated the results with the electrical characteristics of the devices. The STEM examination of the FIB-cross-sectioned devices revealed that at 550 °C the silicon starts to out-diffuse from the nanowire and react with the adjacent titanium layer. After the 750 °C anneal the Si out-diffusion led to two remarkable morphological features: (a) formation of a ∼50 nm thick Ti based silicide layer adjacent to the nanowire, and (b) formation of Kirkendall-effect-induced voids in SiNW. Complete void formation at 850 °C led to significant drop in the yield of the devices. Devices with contacts annealed at 750 °C showed significant improvement in terms of yield and linearity compared to the devices with as-deposited and 450–650 °C annealed contacts. On the other hand, Kirkendall voiding in silicon nanowires was found to be detrimental to the FET performance, possibly causing contact failure at the highest annealing temperature of 850 °C. This study establishes a direct correlation between the thermally induced reactions in the SiNW/metal-contact system and the SiNW FET devices characteristics. These types of studies are crucial for increasing the yield and reliability of nanowire devices.

Acknowledgments

We thank Ritu Bajpai for her help in device fabrication and characterization, and Dr Vladimir P Oleshko of MSEL/NIST for the supplemental TEM images of Si nanowires. The nanowire devices were fabricated at the Nanofab clean room of the NIST Center for Nanoscale Science and Technology. The GMU portion of the work was supported by NSF under ECCS-0901712 grant.

References

[1] Chung S-W, Yu J-Y and Heath J R 2000 *Appl. Phys. Lett.* **76** 2068
[2] Goldberger J, Hochbaum A I, Fan R and Yang P 2006 *Nano Lett.* **6** 973
[3] Zwanenburg F A, Rijmenam C E W M, Fang Y, Lieber C M and Kouwenhoven L P 2009 *Nano Lett.* **9** 1071
[4] Cui Y and Lieber C M 2001 *Science* **291** 851
[5] Hayden O, Agarwal R and Lieber C M 2001 *Nature* **5** 352

[6] Stern E, Klemic J F, Routenberg D A, Wyrembak P N, Turner-Evans D B, Hamilton A D, LaVan D A, Fahmy T M and Reed M A 2007 *Nature* **445** 519
[7] Zheng G, Patolsky F, Cui Y, Wang W U and Lieber C M 2005 *Nat. Biotechnol.* **23** 1294
[8] Tian B, Zheng X, Kempa T J, Fang Y, Yu N, Yu G, Huang J and Lieber C M 2007 *Nature* **449** 885
[9] Hochbaum A I, Chen R, Delgado R D, Liang W, Garnett E C, Najarian M, Majumdar A and Yang P 2008 *Nature* **451** 163
[10] Boukai A I, Bunimovich Y, Tahir-Kheli J, Yu J-K, Goddard W A and Heath J R 2008 *Nature* **451** 168
[11] Appenzeller J, Knoch J, Björk M T, Riel H, Schimd H and Riess W 2008 *IEEE Trans. Electron. Devices* **55** 2827
[12] Ho T-ta, Wang Y, Eichfeld S, Lew K-K, Liu B, Mohney S E, Redwing J M and Mayer T S 2008 *Nano Lett.* **8** 4359
[13] Hayde O, Björk M T, Schimd H, Riel H, Drechsler U, Karg S F, Lörtscher E and Riess W 2007 *Small* **2** 230
[14] Cohen G M, Rooks M J, Chu J O, Laux S E, Solomon J A, Ott J A, Miller R J and Haensch W 2007 *Appl. Phys. Lett.* **90** 233110
[15] Cui Y, Wang D, Wang U W and Lieber C M 2003 *Nano Lett.* **3** 149
[16] Wu Y, Xiang J, Yang C, Lu W and Lieber C M 2004 *Nature* **430** 61
[17] Weber W M *et al* 2006 *Nano Lett.* **6** 2660
[18] Liu B, Wang Y, Dilts S, Mayer T S and Mohney S E 2007 *Nano Lett.* **7** 818
[19] Lin Y-C, Lu K-C, Wu W-W, Bai J, Chen L J, Tu K N and Huang Y 2008 *Nano Lett.* **8** 913
[20] Chen L J 2005 *JOM* **57** 24
[21] Zhang S-L and Smith U 2004 *J. Vac. Sci. Technol.* A **22** 1361
[22] Sze S M 1981 *Physics of Semiconductor Devices* 2nd edn (New York: Wiley)
[23] Mayer J W and Lau S S 1990 *Electronic Material Science: For Integrated Circuits in Si and GaAs* 1st edn (New York: Macmillan)
[24] Schmitt A L, Higgins J M, Szczech J R and Jin S 2010 *J. Mater. Chem.* **20** 223
[25] Speiser R, Naiditch S and Johnston H L 1950 *J. Am. Chem. Soc.* **72** 2578
[26] Kim K-T and Kim C-K 1987 *IEEE Electron. Device Lett.* **8** 569
[27] Motayed A, He M, Davydov A V, Melngailis J and Mohammad S N 2006 *J. Appl. Phys.* **100** 114310
[28] Mayer J, Giannuzzi L A, Kamino T and Michael J 2007 *MRS Bull.* **32** 400
[29] Garnett E C, Liang W and Yang P 2007 *Adv. Mater.* **19** 2946
[30] Ting C Y, Wittmer M, Iyer S S and Brodsky S B 1984 *J. Electrochem. Soc.* **131** 2934
[31] Fast J D 1965 *Interactions of Metals and Gases: Thermodynamics and Phase Relations* (New York: Academic)
[32] Byon K, Tham D, Fischer J E and Johnson A T 2007 *Appl. Phys. Lett.* **90** 143513
[33] Colli A, Pisana S, Fasoli A, Robertson J and Ferrari A C 2007 *Phys. Status Solidi* b **244** 4161
[34] Wunnicke O 2006 *Appl. Phys. Lett.* **89** 083102
[35] Cui Y, Duan X, Hu J and Lieber C M 2000 *J. Phys. Chem.* B **104** 5213
[36] Allen J E *et al* 2008 *Nat. Nanotechnol.* **3** 168
[37] Chen J-W and Milnes A G 1980 *Ann. Rev. Mater. Sci.* **10** 157
[38] Stolwijk N A, Schuster B and Hölzl J 1984 *Appl. Phys.* A **33** 133
[39] Bullis W M 1966 *Solid-State Electron.* **9** 143
[40] Raaijmakers I J and Kim K B 1990 *J. Appl. Phys.* **67** 6255
[41] Fornara P, Denorme S, de Berranger E, Mathiot D, Mouis M and Poncet A 1998 *Microelectron. J.* **29** 71
[42] Holloway K and Sinclair R 1987 *J. Appl. Phys.* **61** 1359
[43] Raaijmakers I J, Reader A H and Oosting P H 1988 *J. Appl. Phys.* **63** 2790
[44] Pey K L, Sundaresan R, Wong H, Siah S Y and Tung C H 2000 *Mater. Sci. Eng.* B **74** 289
[45] Wang M H and Chen L J 1992 *J. Appl. Phys.* **71** 5918
[46] Kim E H, Ko D H, Choi S, Yoo B Y and Lee H D 1999 *J. Electron. Mater.* **28** L20
[47] Cocchi R, Giubertoni R and Ottaviani G 2001 *J. Appl. Phys.* **89** 6079
[48] Chaix-Pluchery O, Chenevier B, Matko I and Sénateur J P 2004 *J. Appl. Phys.* **96** 361
[49] Yang T H, Chi K S and Chen L J 2005 *J. Appl. Phys.* **98** 34302